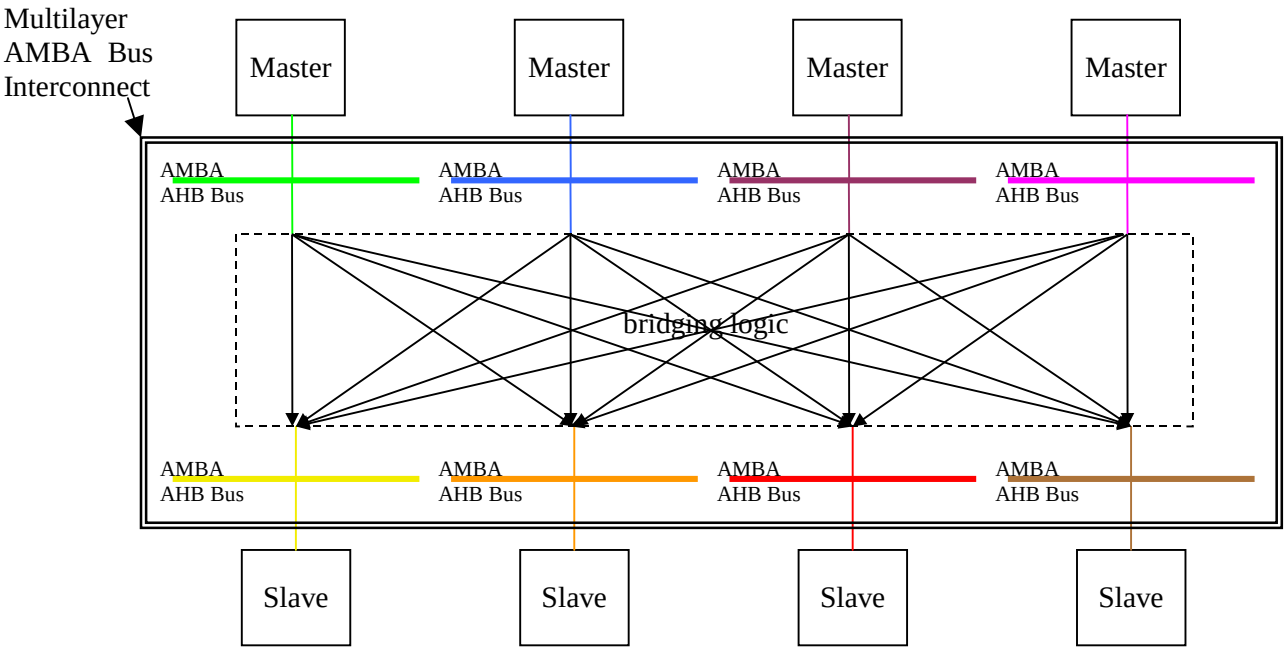
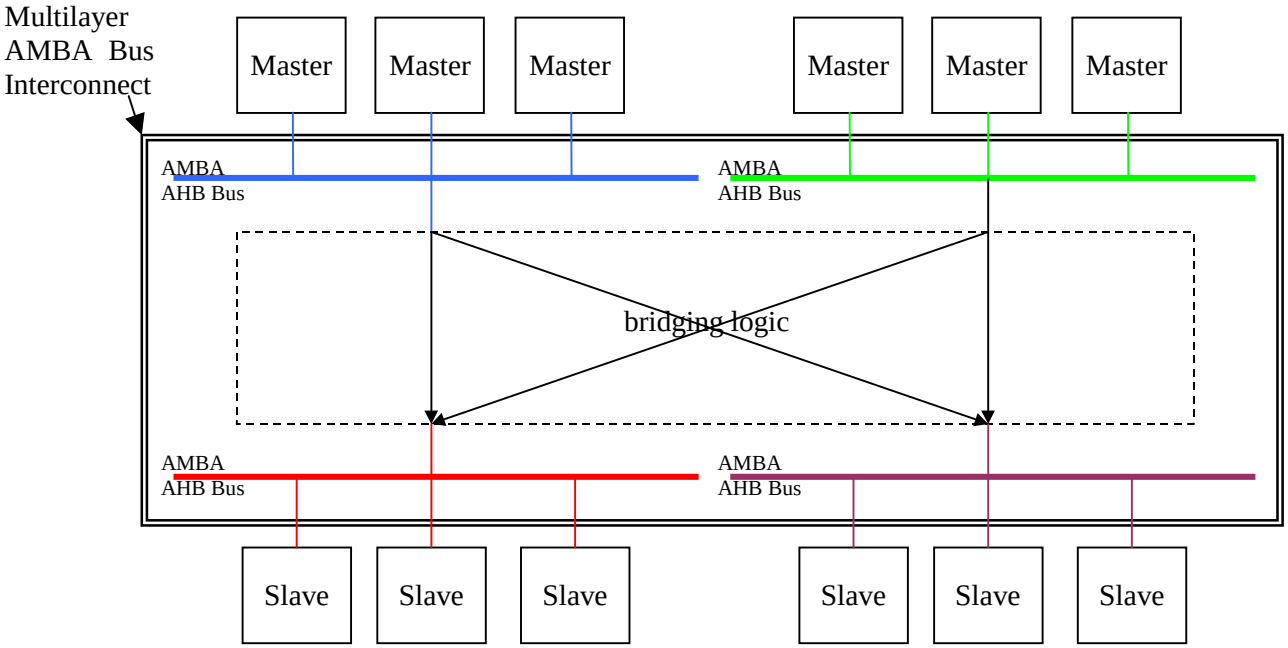
AU-SS4000: Multilayer AMBA Bus Interconnect

The Multilayer AMBA Bus Interconnect provides a configurable multilayer AMBA AHB Bus interconnect. It can be configured as a two to sixteen layer AMBA AHB Bus interconnect. Up to 63 AMBA AHB Bus masters and 63 AMBA AHB Bus slaves can be supported. The read and write data widths are user configurable to either 32 bits or 64 bits. The Multilayer AMBA Bus Interconnect is available as a synthesizable Verilog model from Aurora VLSI, Inc. Contact CustomerService@auroravlsi.com.

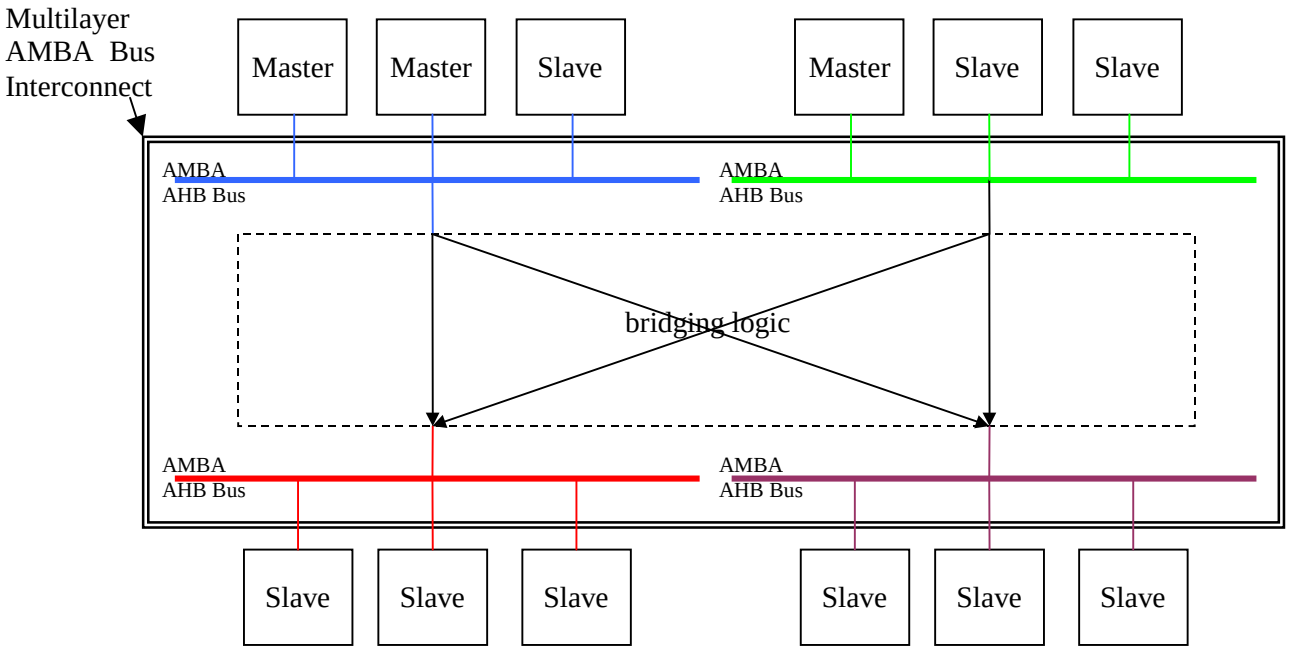
Due to its configurability, the Multilayer AMBA Bus Interconnect is extremely versatile. It can be used in a broad spectrum of applications from relatively simple two bus AMBA AHB systems, to multicore processor systems with extremely high interconnect bandwidth requirements. The following figures give some examples of multilayer AMBA Bus systems using the Multilayer AMBA Bus Interconnect.



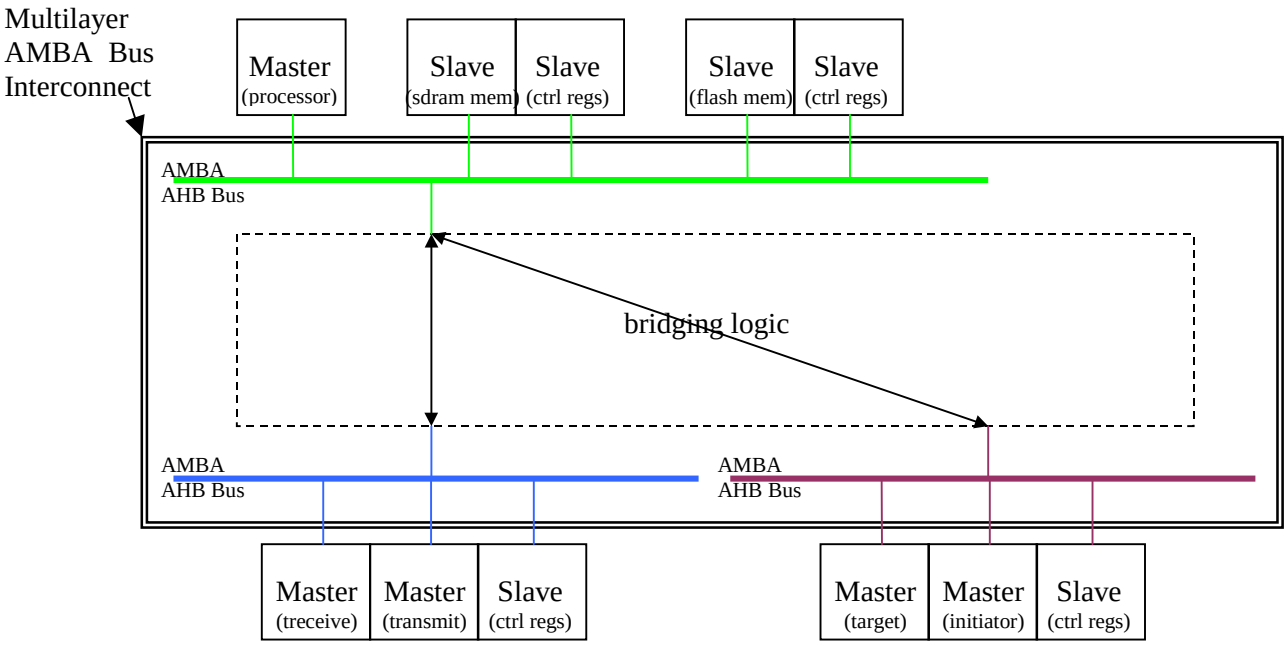
Point to Point Topology From Any Master to Any Slave. One master or slave on each AMBA AHB bus. All slaves are remote (accessed through the Multilayer AMBA Bus Interconnect bridging logic by the masters). Unidirectional bridging logic.



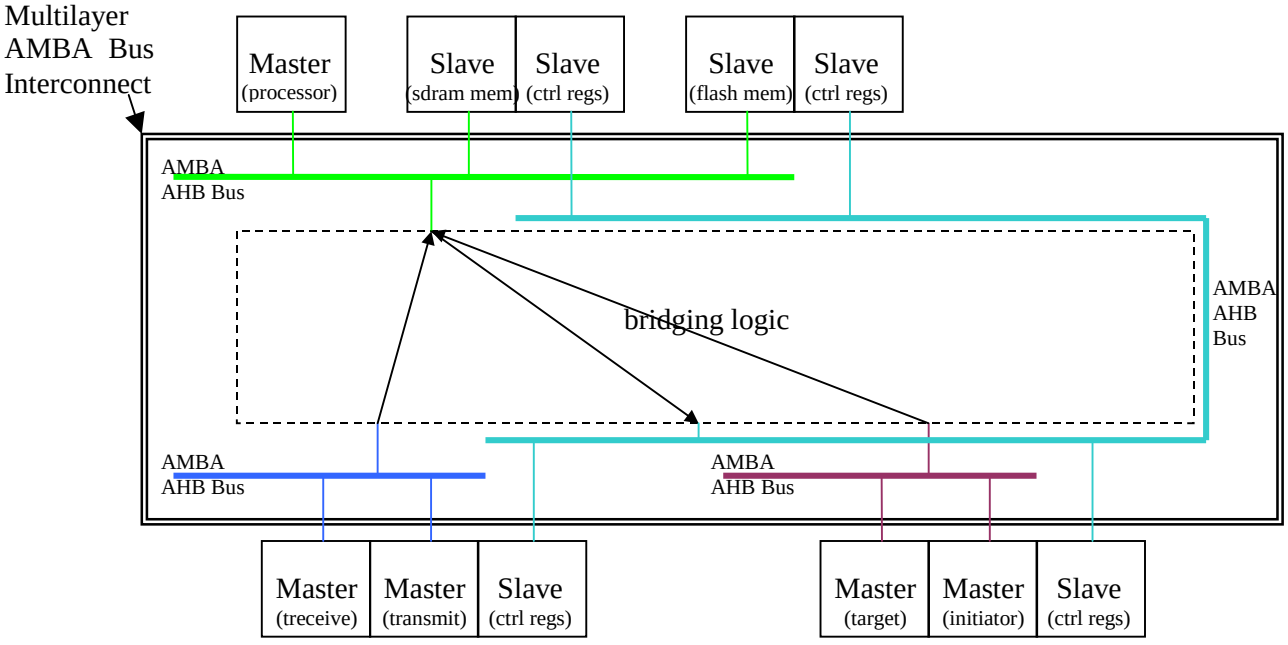
Shared AMBA AHB buses. Multiple masters or slaves on each AMBA AHB bus. All slaves are remote. Unidirectional bridging logic.



Shared AMBA AHB buses. Multiple masters or slaves on each AMBA AHB bus. Remote and local slaves (accessed on the same AMBA AHB bus as the master without going through the Multilayer AMBA Bus Interconnect bridging logic). Unidirectional bridging logic.



Shared AMBA AHB buses. Multiple masters or slaves on each AMBA AHB bus. Remote and local slaves. Bidirectional bridging logic. AMBA AHB peripherals whose DMA masters and control register slaves are on the same bus.



Shared AMBA AHB buses. Multiple masters or slaves on each AMBA AHB bus. Remote and local slaves. Unidirectional bridging logic. Dedicated AMBA AHB control register bus.

Each AMBA AHB Bus of the Multilayer AMBA Bus Interconnect can support up to fifteen AMBA masters and fifteen AMBA slaves that directly connect to it. Additionally, each AMBA AHB Bus can connect to any other AMBA AHB bus over the low latency bridging logic within the Multilayer AMBA Bus Interconnect. AMBA AHB Bus arbiters and decoders that are optimized for the Multilayer AMBA Bus Interconnect are also included for all AMBA AHB Buses.

The Multilayer AMBA Bus Interconnect supports all AMBA AHB response types, including RETRY and SPLIT, along with OKAY and ERROR. This ensures most efficient AMBA Bus usage when there are multiple masters on an AMBA Bus. For example, when data for one master is not ready, that master receives a RETRY response, as opposed to being allowed to hold the bus for an extended time period that would consequently starve the other master(s) on that AMBA Bus.

The bridging logic within the Multilayer AMBA Bus Interconnect includes buffering for read data. Thus, any read that receives a RETRY response due to a slow slave, will be guaranteed to quickly get the read data once the slow slave delivers it to the Multilayer AMBA Bus Interconnect. This feature is a requirement when interfacing to peripherals that have retry timeout time periods that are about the same as latencies of any slow slave that they may access. An example of such a peripheral is a PCI bus controller.

To optimize gate count, the Multilayer AMBA Bus Interconnect is designed so that only the AMBA AHB Bus layers, AMBA master interfaces, AMBA slave interfaces, and bridging logic that is used for the given configuration, is in the synthesized netlist.

Multilayer AMBA Bus Interconnect features are summarized:

- 2 to 16 layer AMBA AHB bus interconnect- user configurable
- 32 bit or 64 bit data widths- user configurable
- 1 to 63 AMBA Bus masters- user configurable
- 1 to 63 AMBA Bus slaves- user configurable
- 0 to 15 AMBA Bus masters per AMBA AHB bus
- 0 to 15 AMBA Bus slaves per AMBA AHB bus
- Fully pipelined for highest throughput
- Low bus to bus latency
- Supports all required AMBA AHB bus features
- Supports all AMBA AHB bus responses- OKAY, ERROR, RETRY, SPLIT
- Unused AMBA AHB bus layers, AMBA Bus master interfaces, AMBA Bus slave interfaces, AMBA Bus address registers, decoders, arbiters, etc. are not in the synthesized netlist to minimize gate count.

The core is delivered as a synthesizeable RTL Verilog model. Deliverables include:

- RTL Verilog source code model of the core
- Verilog testbench and test cases
- Synthesis scripts examples
- Complete detailed documentation and training class notes