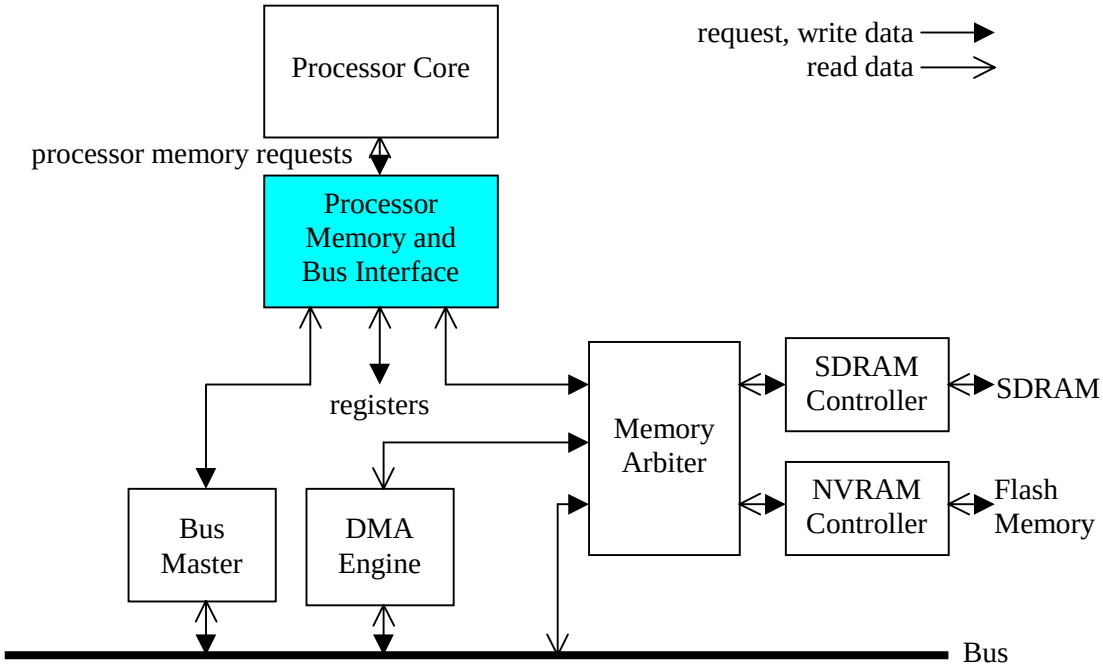
AU-S1000: Processor Memory and Bus Interface Core

The AU-S1000 Processor Memory and Bus Interface Core provides system interfaces for Aurora VLSI processors including the AU-C01XX Processor Core family, AU-J1XXX Java Core family, and AU-J2XXX Java Core family. In an SOC, it connects the Processor Core to the memory system that may include RAM, a system bus, and on-chip control and status registers. The AU-S1000 Processor Memory and Bus Interface Core is available as synthesizable Verilog models from Aurora VLSI, Inc. Contact CustomerService@auroravlsi.com.

The Processor Memory and Bus Interface Core is a block at the Processor Core to memory system interface. It seamlessly connects the Processor Core to the memory system. The figure below shows its usage within an SOC.



The Processor Core issues memory requests on its instruction and data memory interfaces. These two Processor Core memory request interfaces operate independently. The Processor Memory and Bus Interface Core receives these requests, and examines each request address to determine if it is a request for:

- RAM memory
- A system bus peripheral device
- A control or status register within the memory system

It then passes the request information- request address, size, read/write, lock flag, and any write data, to the memory system block that controls the appropriate request target- RAM memory, system bus, or SOC internal control and status registers.

On Processor Core reads, some time after passing the request information to the appropriate request target block, the Processor Memory and Bus Interface receives the read data and error information from the request target block. It then passes this read data and error information back to the Processor Core. The Processor Memory and Bus Interface signals wait cycles to the Processor Core as it waits for the read data and error information.

On Processor Core writes, the Processor Memory and Bus Interface accepts write data with the request. It then passes the write data along with the request to the appropriate memory system target.

Processor Memory and Bus Interface features are summarized:

- Memory and bus interface supporting Aurora VLSI Processor Cores
  - AU-C01XX 32 Bit, Tiny, Low Power Processor Cores
  - AU-JXXXX Java Processor Cores
- Seamless connection to Aurora VLSI Processor Cores
- Memory system requests from the Processor Core on two independent request interfaces
  - instruction request interface
  - data request interface
- Determines the memory request target:
  - RAM memory
  - System bus peripheral device
  - On-chip register
- Drives the request to the memory request target
- Receives read data and error information from the request target
- Passes read data and error information back to the Processor Core
- Signals memory system wait cycles to the Processor Core as needed

The core is delivered as a synthesizeable RTL Verilog model. Deliverables include:

- RTL Verilog source code model of the core
- Verilog testbench and test cases
- Synthesis scripts examples
- Complete detailed documentation and training class notes