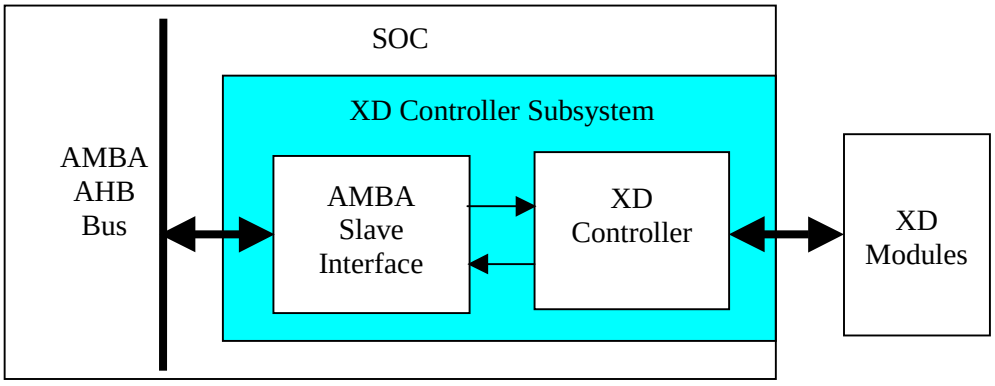
Aurora VLSI

Unleashing the Power of the Internet

AU-MB5000: XD Controller AMBA Subsystem Core

AMBA AHB Bus XD Controller

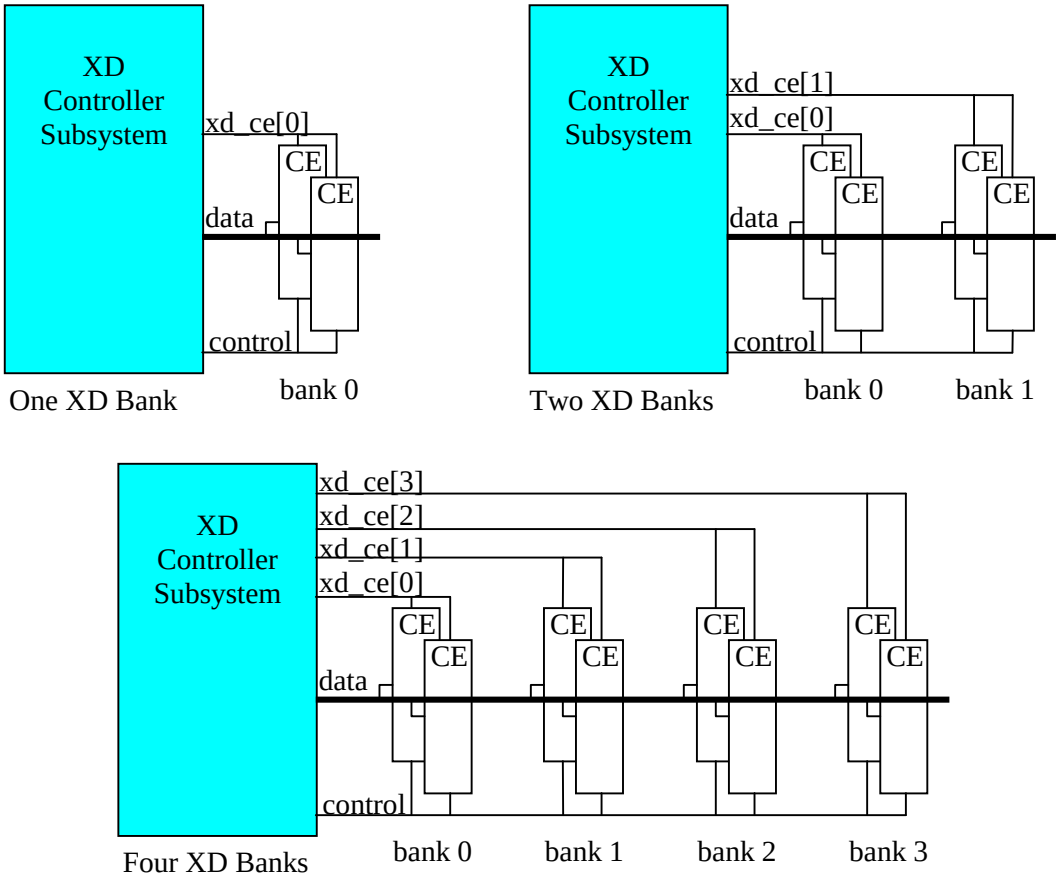
The AU-MB5000 XD Controller AMBA Subsystem provides an XD Controller peripheral subsystem for AMBA based SOCs. It contains an XD Controller that connects seamlessly to the AMBA AHB Bus as an AMBA Bus slave. The XD Controller AMBA Subsystem Core is available as a synthesizable Verilog model from Aurora VLSI, Inc. Contact CustomerService@auroravlsi.com.



The XD Controller Subsystem includes a versatile XD module controller that supports various sizes of XD modules from 16 Mbytes to 8 Gbytes. The XD Controller data bus width is user configurable to 8, 16, or 32 bits. The XD Controller supports XD memory systems from 16 Mbytes to 128 Gbytes. XD module timing parameters are both user configurable at reset with Verilog parameters and software programmable to support a wide range of XD module speed grades and system clock frequencies.

Internal to an SOC, the XD Controller Subsystem is a bus slave peripheral on the AMBA AHB Bus. The XD Controller Subsystem can interface to either a 32 bit or 64 bit AMBA AHB Bus. A Verilog parameter indicates the AMBA Bus width. AMBA Bus transactions that target the XD modules, are recognized by the AMBA Slave Interface of the XD Controller Subsystem. The AMBA Slave Interface initiates XD requests at the requester interface of the XD Controller block. To complete the AMBA Bus transaction, the AMBA Slave Interface drives the appropriate AMBA response onto the AMBA Bus.

The XD Controller Subsystem supports one, two, or four XD banks in XD memory systems through its XD module select outputs- xd_ce[3:0]. The XD data bus and control lines are common to all banks of XD modules.



XD Controller AMBA Subsystem features are summarized:

XD Controller

- 1, 2, or 4 banks of XD modules
- 8 bit, 16 bit, or 32 bit XD Controller data bus
- 16 Mbyte to 128 Gbyte XD memory systems
- User configurable reset values and fully programmable XD module timing parameters
- Read, Program, Erase, Read Status, Read Status2, Read ID, Read ID2, Read ID3, and Reset commands
- 16 Mbyte to 8 Gbyte XD modules- configurable
- 512 byte or 2048 byte page size- configurable
- ECC hardware support
- spare area usage- configurable
- Interrupt or host processor polling for XD command completion

AMBA Slave Interface

- AMBA AHB Bus slave
- 32 bit or 64 bit AMBA AHB Bus- user configurable
- Supports all required AMBA AHB Bus features
- Implements AMBA Bus timeout and RETRY response
- Read data prefetching
- Write data packing
- Same cycle device request/response is supported for highest throughput
- Handles all data packing/unpacking and data alignment for data transfer sizes that do not match the AMBA Bus width and/or XD data bus width
- User configurable for big or little endian AMBA Bus and memory

The core is delivered as a synthesizeable RTL Verilog model. Deliverables include:

- RTL Verilog source code model of the core
- Verilog testbench and test cases
- Synthesis scripts examples
- Complete detailed documentation and training class notes

XD Controller

The XD Controller Subsystem includes the AU-M5000 XD Controller Core. Additional logic at the requester interface of the XD Controller provides an AMBA Bus slave interface, read prefetching logic, and write data packing.

The XD Controller supports the Read, Program, Erase, Read Status, Read Status2, Read ID, Read ID2, Read ID3, and Reset XD commands. ECC support is provided.

Configurable features include page size, data bus width, XD module size, number of XD banks, interrupt enable, ECC functionality, number of address cycles, spare area usage, and address[36:32]. Configurable features have hardwired values upon reset that are user configurable with Verilog parameters. After reset, they can be reconfigured by software. Similarly, XD timing parameters at reset are hardwired to user configurable values. After reset, they are also software programmable.

The host processor initiates XD module operations by writing commands to the XD Controller. When an XD module operation completes, the XD Controller optionally signals a maskable interrupt to the host processor. The host processor may also poll XD Controller registers to determine when an XD module operation has completed.

AMBA Slave Interface

The AMBA Slave Interface of the XD Controller Subsystem, accepts XD requests from the AMBA Bus. The AMBA Slave Interface supports all required AMBA AHB Bus features including all AMBA burst and wrapping types, AMBA sizes up to the AMBA Bus width, and all AMBA Bus responses. When the AMBA Bus data transfer size does not match the AMBA Bus width or XD data bus width, the AMBA Slave Interface packs and/or unpacks the data and aligns the data, for the most efficient transfer of data to/from the XD modules and to/from the AMBA Bus.

The AMBA Slave Interface can respond in the cycle after it receives an AMBA Bus request. This ensures a slave response on the AMBA Bus with no wait states, and therefore highest system performance. To support this fast response time, read data is prefetched whenever possible.

XD modules provide ECC support by including spare memory areas to hold ECC bits. The XD Controller Subsystem can be configured to use this ECC support and do error checking and correction of the single bit correctable errors. This error checking and correction is done in the AMBA Slave Interface.