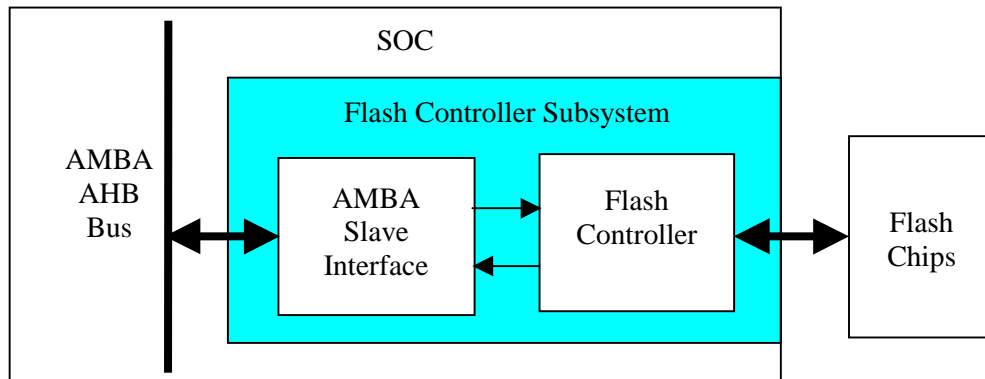


AU-MB3001: Flash Controller AMBA Subsystem Core **AMBA AHB Bus Flash Controller**

The AU-MB3001 Flash Controller AMBA Subsystem provides a Flash Controller peripheral subsystem for AMBA based SOCs. It contains a Flash Controller that connects seamlessly to the AMBA AHB Bus as an AMBA Bus slave. The Flash Controller AMBA Subsystem Core is available as a synthesizable Verilog model from Aurora VLSI, Inc. Contact CustomerService@auroravlsi.com.

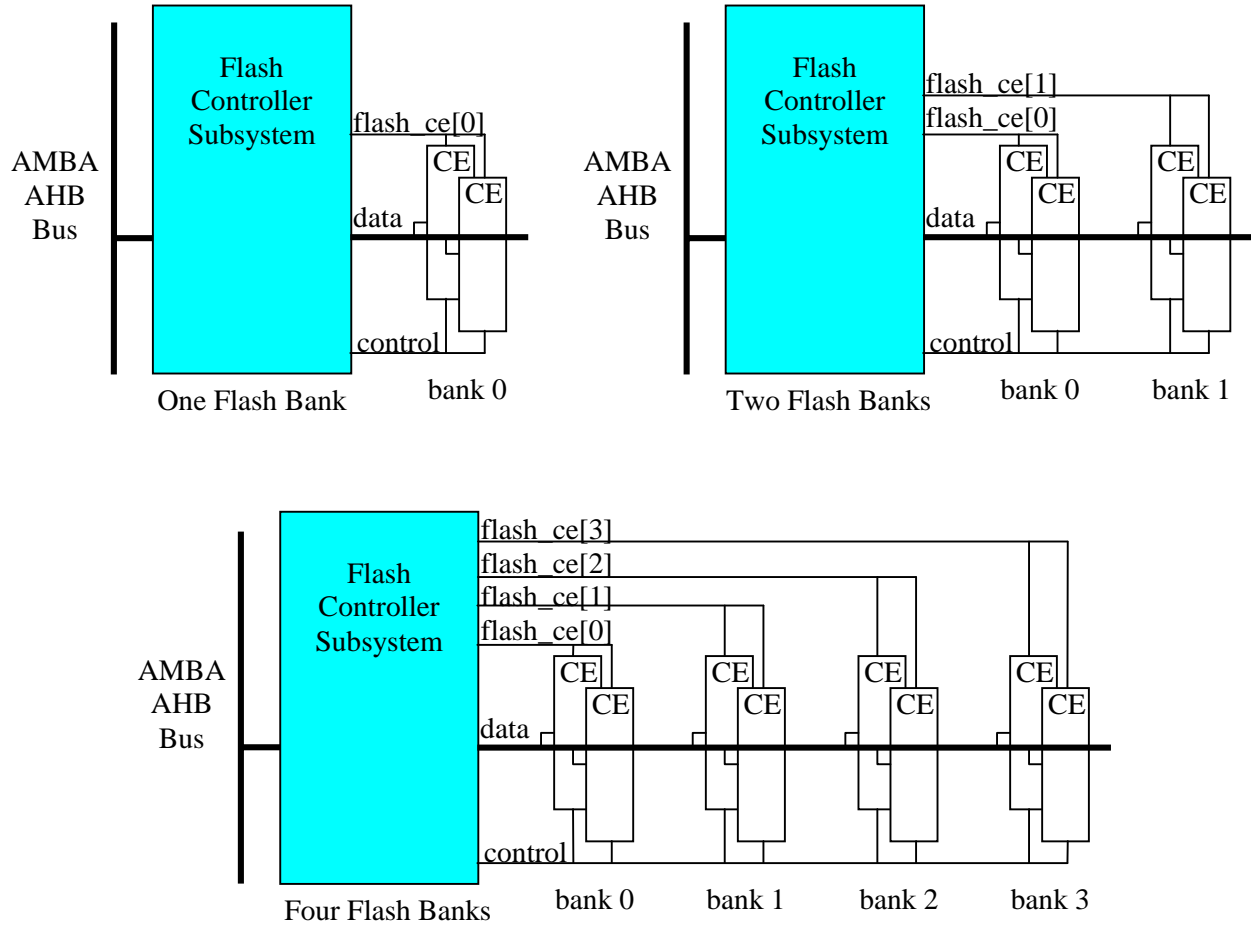


The Flash Controller Subsystem includes a versatile NAND/NOR flash controller that supports various types of NAND and NOR flash chips from several manufacturers. The Flash Controller data bus width is user configurable to 8, 16, 32 or 64 bits. The Flash Controller supports NAND flash memory systems from 8 Mbytes to 512 Gbytes, and NOR flash memory systems from 512 Kbytes to 1 Gbyte. Flash chip timing parameters are both user configurable at reset with Verilog parameters and software programmable to support a wide range of flash speed grades and system clock frequencies.

Internal to an SOC, the Flash Controller Subsystem is a bus slave peripheral on the AMBA AHB Bus. The Flash Controller Subsystem can interface to either a 32 bit or 64 bit AMBA AHB Bus. A Verilog parameter indicates the AMBA Bus width. AMBA Bus transactions that target the flash chips, are recognized by the AMBA Slave Interface of the Flash Controller Subsystem. The AMBA Slave Interface initiates flash requests at the requester interface of the Flash Controller block. To complete the AMBA Bus transaction, the AMBA Slave Interface drives the appropriate AMBA response onto the AMBA Bus.



The Flash Controller Subsystem supports one, two, or four flash banks through its flash chip enable outputs- flash_ce[3:0]. The flash data bus and control lines are common to all flash banks.



Flash Controller AMBA Subsystem features are summarized:

Flash Controller

- NAND and NOR flash controller
- 1, 2, or 4 banks of flash chips
- 8 bit, 16 bit, 32 bit, or 64 bit Flash Controller data bus
- 8 Mbyte to 512 Gbyte NAND flash memory systems
- 512 Kbyte to 1 Gbyte NOR flash memory systems
- User configurable reset values and fully programmable flash chip timing parameters
- NAND flash (SLC and MLC)
 - Read, Program, Erase, Read Status, Read ID, Copy Back, and Reset
 - Other NAND flash commands using Direct Read and Direct Write
 - ONFI industry standard command compatible
 - 64 Mbit to 256 Gbit flash chips- configurable
 - 8 bit or 16 bit flash chip data bus- configurable
 - 512 byte, 2048 byte, or 4096 byte page size- configurable
 - ECC generation and correction
 - spare area usage- configurable
 - 2, 4, or 5 cycle ID register read- configurable
- NOR flash
 - Read, Program, Erase, Read Status, Read ID, Read CFI, Clear Status, Buffered Write, Lock, Unlock, and Lock Down
 - Other NOR flash commands using Direct Read and Direct Write
 - NOR flash RP/RST/RESET (reset) assertion by the Flash Controller Subsystem reset input port
 - 4 Mbit to 512 Mbit flash chips- configurable
 - 8 bit or 16 bit flash chip data bus- configurable
 - 64 Kbyte or 128 Kbyte main block size- configurable
 - top, bottom, or no boot block- configurable
 - 8 Kbyte, 16 Kbyte, or 32 Kbyte boot block size- configurable
- Interrupt or host processor polling for flash command completion

AMBA Slave Interface

- AMBA AHB Bus slave
- 32 bit or 64 bit AMBA AHB Bus- user configurable
- Supports all required AMBA AHB Bus features
- Implements AMBA Bus timeout and RETRY response
- Read data prefetching
- Write data packing
- Same cycle device request/response is supported for highest throughput
- Handles all data packing/unpacking and data alignment for data transfer sizes that do not match the AMBA Bus width and/or flash data bus width
- User configurable for big or little endian AMBA Bus and memory

The core is delivered as a synthesizable RTL Verilog model. Deliverables include:

- RTL Verilog source code model of the core
- Verilog testbench and test cases
- Synthesis scripts examples
- Complete detailed documentation and training class notes

Flash Controller

The Flash Controller Subsystem includes the AU-M3001 Flash Controller Core. Additional logic at the requester interface of the Flash Controller provides an AMBA Bus slave interface, read prefetching logic, and write data packing.

The Flash Controller supports the Read, Program, Erase, Read Status, Read ID, Copy Back, and Reset NAND flash commands. Direct Read and Direct Write commands are used for the less common, special NAND flash accesses, such as OTP accesses. The NAND flash command set is compatible with the ONFI NAND flash industry standard. ECC generation and correction is provided for NAND flash systems. NOR flash commands that are supported include Read, Program, Erase, Read Status, Read ID, Read CFI, Clear Status, Buffered Write, Lock, Unlock, and Lock Down. Additionally, a Direct Read and Direct Write command are provided to access NOR flash chips at arbitrary addresses and with arbitrary write data so that any other NOR flash chip command sequences can be used.

In NAND flash systems, configurable features include page size, data bus width, flash chip size, number of flash banks, interrupt enable, ECC functionality, copy back functionality, command confirmation, number of address cycles, number of ID read cycles, and spare area usage. Configurable features for NOR flash systems include, data bus width, flash chip size, number of flash banks, interrupt enable, block size, boot block configuration, lock feature, burst read feature, buffered write feature, and the CFI feature. Configurable features have hardwired values upon reset that are user configurable with Verilog parameters. After reset, they can be reconfigured by software.

Flash timing parameters at reset are hardwired to user configurable values. After reset, they are software programmable. This allows the Flash Controller to be used for boot code at reset with a wide range of flash speed grades and system cycle times. After booting, performance can be optimized by reconfiguring the flash timing parameters for the specific flash chips that are used and the system clock frequency.

The host processor initiates flash chip operations by writing commands to the Flash Controller. When a flash chip operation completes, the Flash Controller optionally signals a maskable interrupt to the host processor. The host processor may also poll Flash Controller registers to determine when a flash chip operation has completed.

AMBA Slave Interface

The AMBA Slave Interface of the Flash Controller Subsystem, accepts flash requests from the AMBA Bus. The AMBA Slave Interface supports all required AMBA AHB Bus features including all AMBA burst and wrapping types, AMBA sizes up to the AMBA Bus width, and all AMBA Bus responses. When the AMBA Bus data transfer size does not match the AMBA Bus width or flash data bus width the AMBA Slave Interface packs and/or unpacks the data and aligns the data, for the most efficient transfer of data to/from the flash chips and to/from the AMBA Bus.

The AMBA Slave Interface can respond in the cycle after it receives an AMBA Bus request. This ensures a slave response on the AMBA Bus with no wait states, and therefore highest system performance. To support this fast response time, read data is prefetched whenever possible.

NAND flash chips provide ECC support by including spare memory areas to hold ECC bits. The Flash Controller Subsystem can be configured to use this ECC support and do error checking and correction of the single bit correctable errors. This error checking and correction is done in the AMBA Slave Interface.