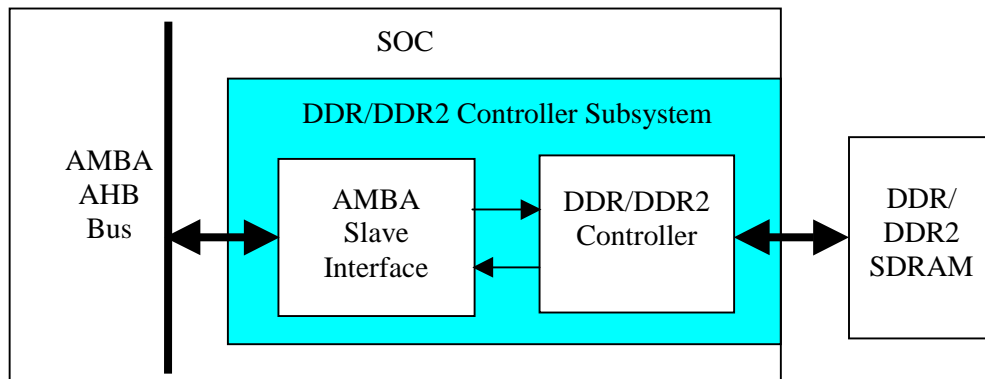




AU-MB2210: DDR/DDR2 Controller AMBA Subsystem **Core**

AMBA AHB Bus DDR/DDR2 Controller

The AU-MB2210 DDR/DDR2 Controller AMBA Subsystem provides a DDR/DDR2 Controller peripheral subsystem for AMBA based SOCs. It contains a DDR/DDR2 Controller that connects seamlessly to the AMBA AHB Bus as an AMBA Bus slave. The DDR/DDR2 Controller AMBA Subsystem Core is available as a synthesizable Verilog model from Aurora VLSI, Inc. Contact CustomerService@auroravlsi.com.

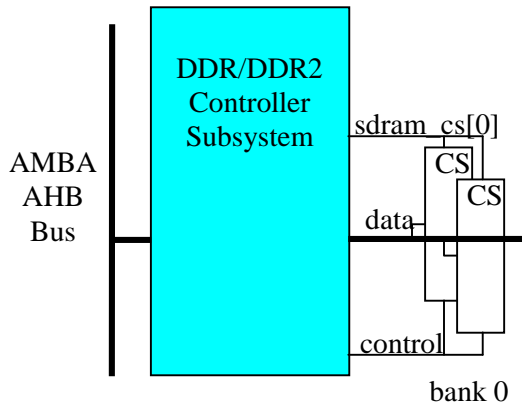


The DDR/DDR2 Controller Subsystem includes a pipelined, high performance DDR/DDR2 Controller. The DDR/DDR2 SDRAM data bus width is user configurable to 32 or 64 bits. The DDR/DDR2 Controller supports DDR and DDR2 SDRAM memory systems from 4 Mbytes to 4 Gbytes. DDR/DDR2 SDRAM timing parameters are software programmable to support a wide range of DDR and DDR2 SDRAM speed grades and clock frequencies. Refresh is initiated by the DDR/DDR2 Controller according to the software programmable refresh interval. To conserve power the DDR/DDR2 SDRAMs can be put in low power mode.

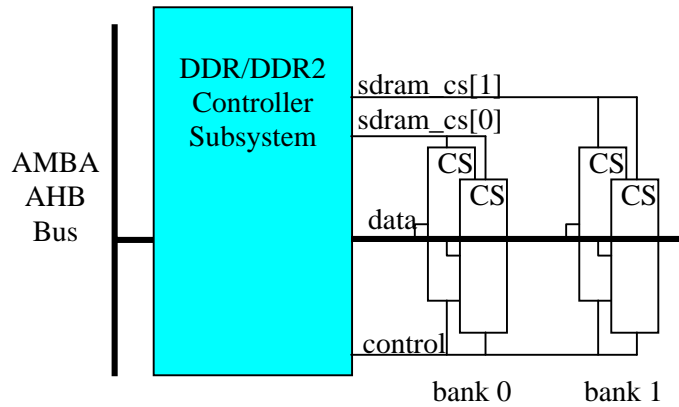
Internal to an SOC, the DDR/DDR2 Controller Subsystem is a bus slave peripheral on the AMBA AHB Bus. The DDR/DDR2 Controller Subsystem can interface to either a 32 bit or 64 bit AMBA AHB Bus. A Verilog parameter indicates the AMBA Bus width. AMBA Bus transactions that target the DDR/DDR2 SDRAMs, are recognized by the AMBA Slave Interface of the DDR/DDR2 Controller Subsystem. The AMBA Slave Interface then initiates a DDR/DDR2 SDRAM request at the requester interface of the DDR/DDR2 Controller block. To complete the transaction, the AMBA Slave Interface drives the appropriate AMBA response onto the AMBA Bus.



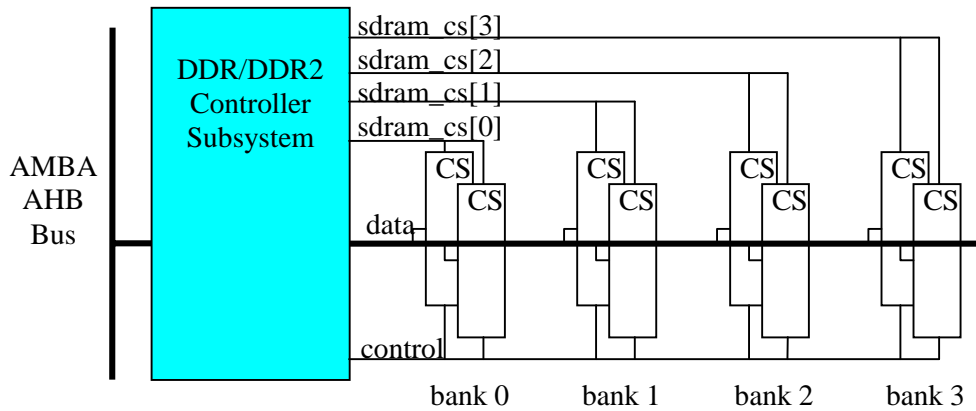
The DDR/DDR2 Controller Subsystem supports one, two, or four DDR/DDR2 SDRAM banks (external banks) in DDR and DDR2 SDRAM memory systems through its DDR/DDR2 SDRAM chip select outputs- sdr_m_cs[3:0]. The DDR/DDR2 SDRAM data bus, control lines, and clock are common to all banks of DDR/DDR2 SDRAM.



One DDR/DDR2 SDRAM Bank



Two DDR/DDR2 SDRAM Banks



Four DDR/DDR2 SDRAM Banks



DDR/DDR2 Controller AMBA Subsystem features are summarized:

DDR/DDR2 Controller

- 32 bit or 64 bit DDR/DDR2 SDRAM data bus
- 4 Mbyte to 4 Gbyte DDR/DDR2 memory system
- Pipelined accesses to active rows for highest performance
- 1, 2, or 4 banks of DDR/DDR2 SDRAMs
- DDR/DDR2 SDRAM powerdown supported
- Fully programmable DDR/DDR2 SDRAM timing parameters
- Auto-refresh with programmable DDR/DDR2 SDRAM refresh interval
- DDR
 - 2, 2.5, or 3 cycle CAS latency
 - 4 DDR SDRAM internal banks
 - 9, 10, 11, or 12 column address bits
 - 12, 13, or 14 row address bits
- DDR2
 - 3, 4, or 5 cycle CAS latency
 - 4 or 8 DDR/DDR2 SDRAM internal banks
 - 9, 10, 11, or 12 column address bits
 - 13 or 14 row address bits

AMBA Slave Interface

- AMBA AHB Bus slave
- 32 bit or 64 bit AMBA AHB Bus- user configurable
- Supports all required AMBA AHB Bus features
- Implements AMBA Bus timeout and RETRY response
- Read data prefetching
- Write data packing
- Same cycle device request/response is supported for highest throughput
- Handles all data packing/unpacking and data alignment for data transfer sizes that do not match the AMBA Bus width and/or DDR/DDR2 SDRAM data bus width
- User configurable for big or little endian AMBA Bus and memory
- AMBA Bus and DDR/DDR2 SDRAM interface can be asynchronous to each other

The core is delivered as a synthesizable RTL Verilog model. Deliverables include:

- RTL Verilog source code model of the core
- Verilog testbench and test cases
- Synthesis scripts examples
- Complete detailed documentation and training class notes



DDR/DDR2 Controller

The DDR/DDR2 Controller Subsystem includes the AU-M2210 DDR/DDR2 Controller Core. Additional logic at the requester interface of the DDR/DDR2 Controller provides an AMBA Bus slave interface, read prefetching logic, and write data packing.

The DDR/DDR2 Controller accepts DDR and DDR2 SDRAM requests from the AMBA Slave Interface, and compares the request address to addresses of all active rows. If the request address falls in an active row, the request goes directly to the DDR/DDR2 SDRAMs without stalling the DDR/DDR2 Controller pipeline. This results in a peak bandwidth of 4 bytes/cycle with a 32 bit DDR/DDR2 SDRAM data bus, and 8 bytes/cycle with a 64 bit DDR/DDR2 SDRAM data bus. Once a row is activated, it is left activated so that the maximum amount of requests are to active rows, resulting in highest performance.

The number of row address bits, column address bits, bank address bits, and DDR/DDR2 SDRAM banks is software configurable. Nine to twelve column address bits are supported. The number of row address bits can be set to twelve, thirteen, or fourteen. DDR SDRAMs with four internal banks are supported. DDR2 SDRAMs with four or eight internal banks are supported. One, two, or four banks of DDR/DDR2 SDRAMs (external banks) can be built into the system. The DDR/DDR2 SDRAM chip select pins are used to identify the accessed bank of DDR/DDR2 SDRAM. This flexibility permits DDR/DDR2 SDRAM memory system of 4 Mbytes to 4 Gbytes.

DDR/DDR2 SDRAM timing parameters are software programmable. This allows the DDR/DDR2 Controller to be used with a wide range of DDR and DDR2 SDRAM speed grades and cycle times. CAS latency, DDR/DDR2 SDRAM drive strength, and ODT RTT (DDR2 only) are also software programmable.

The DDR/DDR2 SDRAM refresh interval is software programmable. Each time the refresh interval expires, the DDR/DDR2 Controller performs an auto-refresh cycle to all DDR/DDR2 SDRAM internal and external banks.

Upon reset, DDR and DDR2 SDRAM accesses are disabled. After programming the DDR/DDR2 Controller registers to configure the DDR/DDR2 SDRAM system- DDR or DDR2, sizes, timing parameters, CAS latency, etc., software enables DDR/DDR2 SDRAM accesses. Once enabled, the DDR/DDR2 Controller loads the DDR/DDR2 SDRAMs' Mode Registers, performs the appropriate refresh cycles, and is then ready to accept DDR/DDR2 SDRAM read and write requests.

The user may put the DDR/DDR2 SDRAMs into low power mode through software. The DDR/DDR2 Controller continues to initiate refresh cycles while the DDR/DDR2 SDRAMs are powered down. Low power mode is exited when a read/write request occurs or when software exits low power mode.



AMBA Slave Interface

The AMBA Slave Interface of the DDR/DDR2 Controller Subsystem, accepts DDR and DDR2 SDRAM requests from the AMBA Bus. The AMBA Slave Interface supports all required AMBA AHB Bus features including all AMBA burst and wrapping types, AMBA sizes up to the AMBA Bus width, and all AMBA Bus responses. When the AMBA Bus data transfer size does not match the AMBA Bus width or DDR/DDR2 SDRAM data bus width, the AMBA Slave Interface packs and/or unpacks the data and aligns the data, for the most efficient transfer of data to/from the DDR/DDR2 SDRAMs and to/from the AMBA Bus.

The AMBA Slave Interface can respond in the cycle after it receives an AMBA Bus request. This ensures a slave response on the AMBA Bus with no wait states, and therefore highest system performance. To support this fast response time, read data is prefetched whenever possible.

Typically, the DDR/DDR2 SDRAMs and the AMBA Bus do not run at the same clock rate. The AMBA Bus and DDR/DDR2 SDRAM interface can be completely asynchronous to each other due to the two independent clock domains of the DDR/DDR2 Controller Subsystem. One clock domain includes the AMBA Bus interface logic. The DDR/DDR2 SDRAM interface logic is in the second clock domain. These two clock domains come together in the AMBA Slave Interface block. Each clock domain has its own DDR/DDR2 Controller Subsystem clock input.