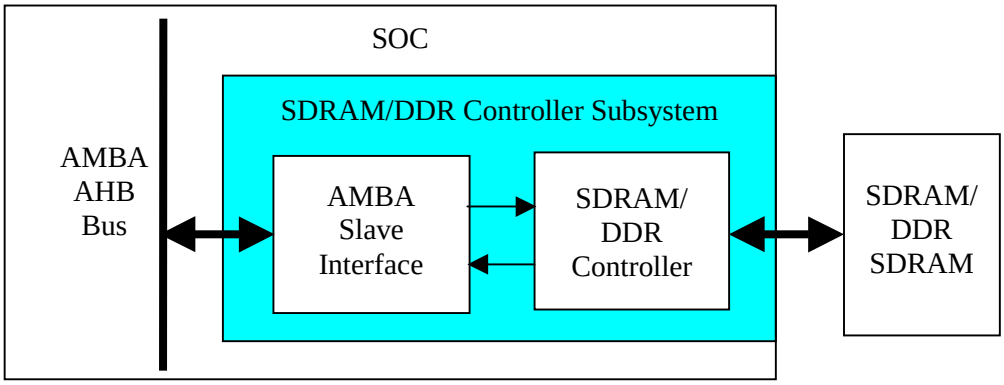
AU-MB2200: SDRAM/DDR Controller AMBA Subsystem Core

AMBA AHB Bus SDRAM/DDR Controller

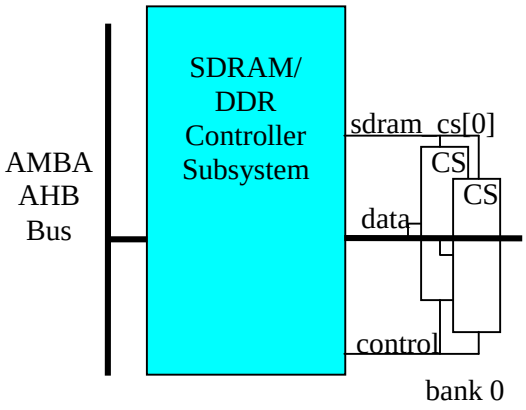
The AU-MB2200 SDRAM/DDR Controller AMBA Subsystem provides an SDRAM/DDR Controller peripheral subsystem for AMBA based SOCs. It contains an SDRAM/DDR Controller that connects seamlessly to the AMBA AHB Bus as an AMBA Bus slave. The SDRAM/DDR Controller AMBA Subsystem Core is available as a synthesizable Verilog model from Aurora VLSI, Inc. Contact CustomerService@auroravlsi.com.



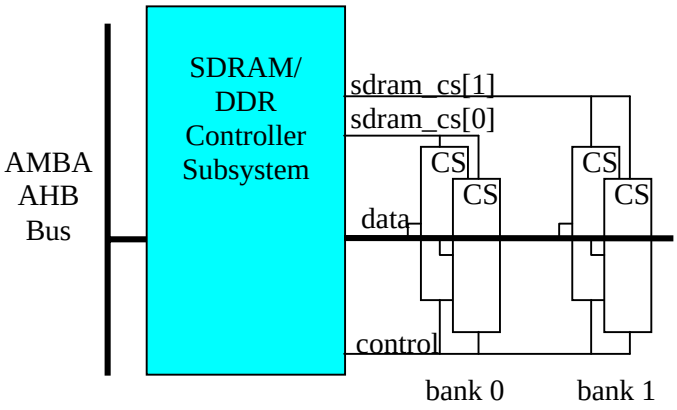
The SDRAM/DDR Controller Subsystem includes a pipelined, high performance SDRAM/DDR Controller. The SDRAM/DDR SDRAM data bus width is user configurable to 32 or 64 bits. The SDRAM/DDR Controller supports SDRAM and DDR SDRAM memory systems from 4 Mbytes to 4 Gbytes. SDRAM/DDR SDRAM timing parameters are software programmable to support a wide range of SDRAM and DDR SDRAM speed grades and clock frequencies. Refresh is initiated by the SDRAM/DDR Controller according to the software programmable refresh interval. To conserve power the SDRAM/DDR SDRAMs can be put in low power mode.

Internal to an SOC, the SDRAM/DDR Controller Subsystem is a bus slave peripheral on the AMBA AHB Bus. The SDRAM/DDR Controller Subsystem can interface to either a 32 bit or 64 bit AMBA AHB Bus. A Verilog parameter indicates the AMBA Bus width. AMBA Bus transactions that target the SDRAM/DDR SDRAMs, are recognized by the AMBA Slave Interface of the SDRAM/DDR Controller Subsystem. The AMBA Slave Interface then initiates an SDRAM/DDR SDRAM request at the requester interface of the SDRAM/DDR Controller block. To complete the transaction, the AMBA Slave Interface drives the appropriate AMBA response onto the AMBA Bus.

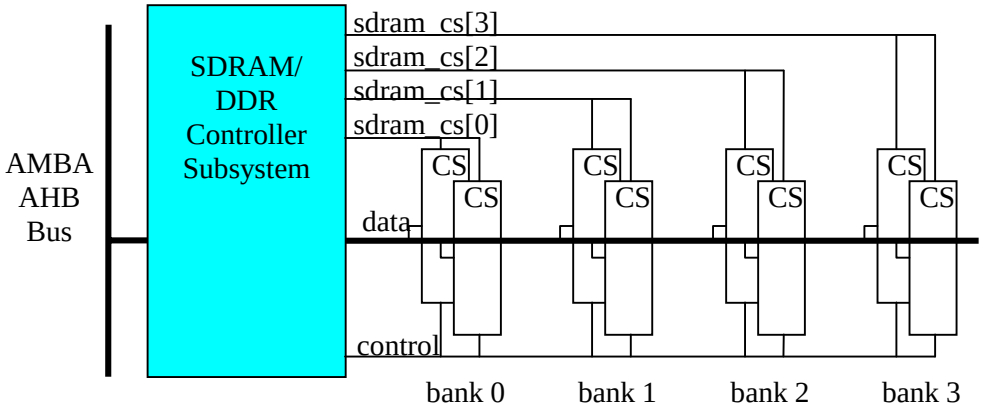
The SDRAM/DDR Controller Subsystem supports one, two, or four SDRAM/DDR SDRAM banks (external banks) in SDRAM and DDR SDRAM memory systems through its SDRAM/DDR SDRAM chip select outputs- sdram_cs[3:0]. The SDRAM/DDR SDRAM data bus, control lines, and clock are common to all banks of SDRAM/DDR SDRAM.



One SDRAM/DDR SDRAM Bank



Two SDRAM/DDR SDRAM Banks



Four SDRAM/DDR SDRAM Banks

SDRAM/DDR Controller AMBA Subsystem features are summarized:

SDRAM/DDR Controller

- 32 bit or 64 bit SDRAM/DDR SDRAM data bus
- 4 Mbyte to 4 Gbyte SDRAM/DDR memory system
- Pipelined accesses to active rows for highest performance
- 1, 2, or 4 banks of SDRAM/DDR SDRAMs
- SDRAM/DDR SDRAM powerdown supported
- Fully programmable SDRAM/DDR SDRAM timing parameters
- Auto-refresh with programmable SDRAM/DDR SDRAM refresh interval
- SDRAM
  - 2 or 3 cycle CAS latency
  - 2 or 4 SDRAM internal banks
  - 8, 9, 10, 11, or 12 column address bits
  - 11, 12, or 13 row address bits
- DDR
  - 2, 2.5, or 3 cycle CAS latency
  - 4 DDR SDRAM internal banks
  - 9, 10, 11, or 12 column address bits
  - 12, 13, or 14 row address bits

AMBA Slave Interface

- AMBA AHB Bus slave
- 32 bit or 64 bit AMBA AHB Bus- user configurable
- Supports all required AMBA AHB Bus features
- Implements AMBA Bus timeout and RETRY response
- Read data prefetching
- Write data packing
- Same cycle device request/response is supported for highest throughput
- Handles all data packing/unpacking and data alignment for data transfer sizes that do not match the AMBA Bus width and/or SDRAM/DDR SDRAM data bus width
- User configurable for big or little endian AMBA Bus and memory
- AMBA Bus and SDRAM/DDR SDRAM interface can be asynchronous to each other

The core is delivered as a synthesizeable RTL Verilog model. Deliverables include:

- RTL Verilog source code model of the core
- Verilog testbench and test cases
- Synthesis scripts examples
- Complete detailed documentation and training class notes

SDRAM/DDR Controller

The SDRAM/DDR Controller Subsystem includes the AU-M2200 SDRAM/DDR Controller Core. Additional logic at the requester interface of the SDRAM/DDR Controller provides an AMBA Bus slave interface, read prefetching logic, and write data packing.

The SDRAM/DDR Controller accepts SDRAM and DDR SDRAM requests from the AMBA Slave Interface, and compares the request address to addresses of all active rows. If the request address falls in an active row, the request goes directly to the SDRAM/DDR SDRAMs without stalling the SDRAM/DDR Controller pipeline. This results in a peak bandwidth of 4 bytes/cycle with a 32 bit SDRAM/DDR SDRAM data bus, and 8 bytes/cycle with a 64 bit SDRAM/DDR SDRAM data bus. Once a row is activated, it is left activated so that the maximum amount of requests are to active rows, resulting in highest performance.

The number of row address bits, column address bits, bank address bits, and SDRAM/DDR SDRAM banks is software configurable. Eight to twelve column address bits are supported. The number of row address bits can be set to eleven, twelve, thirteen, or fourteen. SDRAMs with either two or four internal banks are supported. DDR SDRAMs with four internal banks are supported. One, two, or four banks of SDRAM/DDR SDAMs (external banks) can be built into the system. The SDRAM/DDR SDRAM chip select pins are used to identify the accessed bank of SDRAM/DDR SDRAM. This flexibility permits SDRAM/DDR SDRAM memory system of 4 Mbytes to 4 Gbytes.

SDRAM/DDR SDRAM timing parameters are software programmable. This allows the SDRAM/DDR Controller to be used with a wide range of SDRAM and DDR SDRAM speed grades and cycle times. CAS latency and DDR SDRAM drive strength are also software programmable.

The SDRAM/DDR SDRAM refresh interval is software programmable. Each time the refresh interval expires, the SDRAM/DDR Controller performs an auto-refresh cycle to all SDRAM/DDR SDRAM internal and external banks.

Upon reset, SDRAM and DDR SDRAM accesses are disabled. After programming the SDRAM/DDR Controller registers to configure the SDRAM/DDR SDRAM system- SDRAM or DDR SDRAMs, sizes, timing parameters, CAS latency, etc., software enables SDRAM/DDR SDRAM accesses. Once enabled, the SDRAM/DDR Controller loads the SDRAM/DDR SDRAMs' Mode Registers, performs the appropriate refresh cycles, and is then ready to accept SDRAM/DDR SDRAM read and write requests.

The user may put the SDRAM/DDR SDRAMs into low power mode through software. The SDRAM/DDR Controller continues to initiate refresh cycles while the SDRAM/DDR SDRAMs are powered down. Low power mode is exited when a read/write request occurs or when software exits low power mode.

AMBA Slave Interface

The AMBA Slave Interface of the SDRAM/DDR Controller Subsystem, accepts SDRAM and DDR SDRAM requests from the AMBA Bus. The AMBA Slave Interface supports all required AMBA AHB Bus features including all AMBA burst and wrapping types, AMBA sizes up to the AMBA Bus width, and all AMBA Bus responses. When the AMBA Bus data transfer size does not match the AMBA Bus width or SDRAM/DDR SDRAM data bus width, the AMBA Slave Interface packs and/or unpacks the data and aligns the data, for the most efficient transfer of data to/from the SDRAM/DDR SDRAMs and to/from the AMBA Bus.

The AMBA Slave Interface can respond in the cycle after it receives an AMBA Bus request. This ensures a slave response on the AMBA Bus with no wait states, and therefore highest system performance. To support this fast response time, read data is prefetched whenever possible.

Typically, the SDRAM/DDR SDRAMs and the AMBA Bus do not run at the same clock rate. The AMBA Bus and SDRAM/DDR SDRAM interface can be completely asynchronous to each other due to the two independent clock domains of the SDRAM/DDR Controller Subsystem. One clock domain includes the AMBA Bus interface logic. The SDRAM/DDR SDRAM interface logic is in the second clock domain. These two clock domains come together in the AMBA Slave Interface block. Each clock domain has its own SDRAM/DDR Controller Subsystem clock input.