AU-M5000: XD Controller Core

The AU-M5000 XD Controller Core is a versatile XD module controller that supports various sizes of XD modules from 16 Mbytes to 8 Gbytes. The XD Controller data bus width is user configurable to 8, 16, or 32 bits. The XD Controller supports XD memory systems from 16 Mbytes to 128 Gbytes. XD module timing parameters are both user configurable at reset with Verilog parameters and software programmable to support a wide range of XD module speed grades and system clock frequencies. The XD Controller is available as a synthesizable Verilog model from Aurora VLSI, Inc. Contact CustomerService@auroravlsi.com.

The XD Controller supports the Read, Program, Erase, Read Status, Read Status2, Read ID, Read ID2, Read ID3, and Reset XD commands. ECC support is provided.

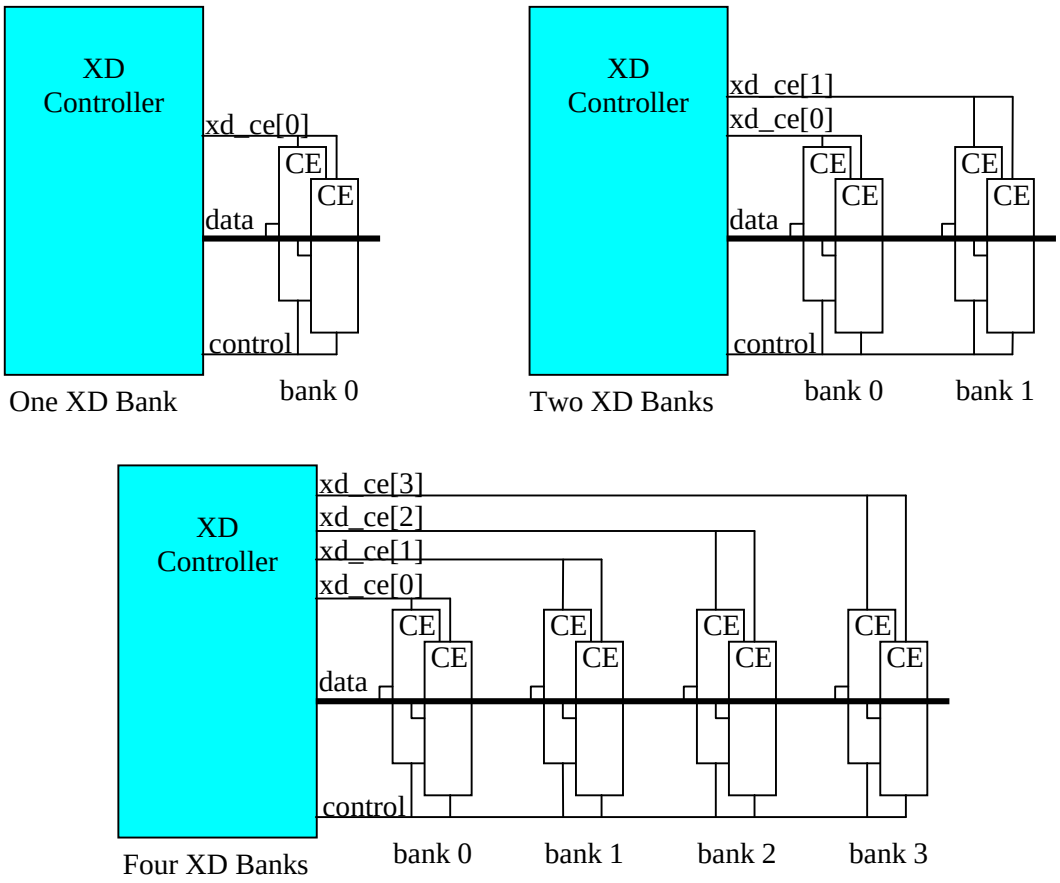
Configurable features include page size, data bus width, XD module size, number of XD banks, interrupt enable, ECC functionality, number of address cycles, spare area usage, and address[36:32]. Configurable features have hardwired values upon reset that are user configurable with Verilog parameters. After reset, they can be reconfigured by software. Similarly, XD timing parameters at reset are hardwired to user configurable values. After reset, they are also software programmable.

The host processor initiates XD module operations by writing commands to the XD Controller. When an XD module operation completes, the XD Controller optionally signals a maskable interrupt to the host processor. The host processor may also poll XD Controller registers to determine when an XD module operation has completed.

XD Controller features are summarized:

- 1, 2, or 4 banks of XD modules
- 8 bit, 16 bit, or 32 bit XD Controller data bus
- 16 Mbyte to 128 Gbyte XD memory systems
- User configurable reset values and fully programmable XD module timing parameters
- Read, Program, Erase, Read Status, Read Status2, Read ID, Read ID2, Read ID3, and Reset commands
- 16 Mbyte to 8 Gbyte XD modules- configurable
- 512 byte or 2048 byte page size- configurable
- ECC hardware support
- spare area usage- configurable
- Interrupt or host processor polling for XD command completion

The XD Controller supports one, two, or four XD banks in XD memory systems through its XD module select outputs- xd_ce[3:0]. The XD data bus and control lines are common to all banks of XD modules.



The core is delivered as a synthesizeable RTL Verilog model. Deliverables include:

- RTL Verilog source code model of the core
- Verilog testbench and test cases
- Synthesis scripts examples
- Complete detailed documentation and training class notes