AU-M2300: SDRAM/DDR/DDR2 Controller Core

The AU-M2300 SDRAM/DDR/DDR2 Controller Core is a pipelined, high performance SDRAM, DDR, and DDR2 SDRAM controller. Software configures the SDRAM/DDR/DDR2 Controller for one of SDRAM, DDR, or DDR2 SDRAM accesses. The SDRAM/DDR/DDR2 SDRAM data bus width is user configurable to 32 or 64 bits. The SDRAM/DDR/DDR2 Controller supports SDRAM, DDR, and DDR2 SDRAM memory systems from 4 Mbytes to 4 Gbytes. SDRAM/DDR/DDR2 SDRAM timing parameters are software programmable to support a wide range of SDRAM, DDR, and DDR2 SDRAM speed grades and clock frequencies. Refresh is initiated by the SDRAM/DDR/DDR2 Controller according to the software programmable refresh interval. To conserve power the SDRAM/DDR/DDR2 SDRAMs can be put in low power mode. The SDRAM/DDR/DDR2 Controller is available as a synthesizable Verilog model from Aurora VLSI, Inc. Contact CustomerService@auroravlsi.com.

The SDRAM/DDR/DDR2 Controller accepts SDRAM, DDR, and DDR2 SDRAM requests and compares the request address to addresses of all active rows. If the request address falls in an active row, the request goes directly to the SDRAM/DDR/DDR2 SDRAMs without stalling the SDRAM/DDR/DDR2 Controller pipeline. This results in a peak bandwidth of 4 bytes/cycle with a 32 bit SDRAM/DDR/DDR2 SDRAM data bus, and 8 bytes/cycle with a 64 bit SDRAM/DDR/DDR2 SDRAM data bus. Once a row is activated, it is left activated so that the maximum amount of requests are to active rows, resulting in highest performance.

The number of row address bits, column address bits, bank address bits, and SDRAM/DDR/DDR2 SDRAM banks is software configurable. Eight to twelve column address bits are supported. The number of row address bits can be set to eleven, twelve, thirteen, or fourteen. SDRAMs with either two or four intrnal banks are supported. DDR SDRAMs with four internal banks are supported. DDR2 SDRAMs with four or eight internal banks are supported. One, two, or four banks of SDRAM/DDR/DDR2 SDAMs (external banks) can be built into the system. The SDRAM/DDR/DDR2 SDRAM chip select pins are used to identify the accessed bank of SDRAM/DDR/DDR2 SDRAM. This flexibility permits SDRAM/DDR/DDR2 SDRAM memory system of 4 Mbytes to 4 Gbytes.

SDRAM/DDR/DDR2 SDRAM timing parameters are software programmable. This allows the SDRAM/DDR/DDR2 Controller to be used with a wide range of SDRAM, DDR, and DDR2 SDRAM speed grades and cycle times. CAS latency, DDR/DDR2 SDRAM drive strength, and ODT RTT (DDR2 only) are also software programmable.

The SDRAM/DDR/DDR2 SDRAM refresh interval is software programmable. Each time the refresh interval expires, the SDRAM/DDR/DDR2 Controller performs an auto-refresh cycle to all SDRAM/DDR/DDR2 SDRAM internal and external banks.

Upon reset, SDRAM, DDR, and DDR2 SDRAM accesses are disabled. After programming the SDRAM/DDR/DDR2 Controller registers to configure the SDRAM/DDR/DDR2 SDRAM system- SDRAM, DDR, or DDR2 SDRAMs, sizes, timing parameters, CAS latency, etc., software enables SDRAM/DDR/DDR2 SDRAM accesses. Once enabled, the SDRAM/DDR/DDR2 Controller loads the SDRAM/DDR/DDR2 SDRAMs' Mode Registers, performs the appropriate refresh cycles, and is then ready to accept SDRAM/DDR/DDR2 SDRAM read and write requests.

The user may put the SDRAM/DDR/DDR2 SDRAMs into low power mode through software. The SDRAM/DDR/DDR2 Controller continues to initiate refresh cycles while the SDRAM/DDR/DDR2 SDRAMs are powered down. Low power mode is exited when a read/write request occurs or when software exits low power mode.

SDRAM/DDR/DDR2 Controller features are summarized:

- 32 bit or 64 bit SDRAM/DDR/DDR2 SDRAM data bus
- 4 Mbyte to 4 Gbyte SDRAM/DDR/DDR2 memory system
- Pipelined accesses to active rows for highest performance
- 1, 2, or 4 banks of SDRAM/DDR/DDR2 SDRAMs
- SDRAM/DDR/DDR2 SDRAM powerdown supported
- Fully programmable SDRAM/DDR/DDR2 SDRAM timing parameters
- Auto-refresh with programmable SDRAM/DDR/DDR2 SDRAM refresh interval

SDRAM

- 2 or 3 cycle CAS latency
- 2 or 4 SDRAM internal banks
- 8, 9, 10, 11, or 12 column address bits
- 11, 12, or 13 row address bits

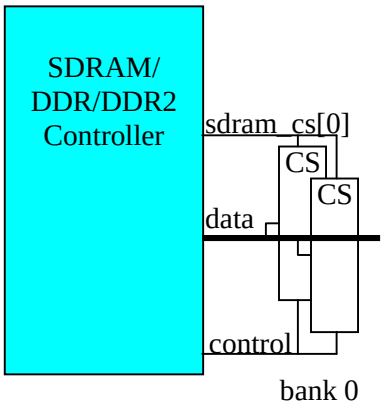
DDR

- 2, 2.5, or 3 cycle CAS latency
- 4 DDR SDRAM internal banks
- 9, 10, 11, or 12 column address bits
- 12, 13, or 14 row address bits

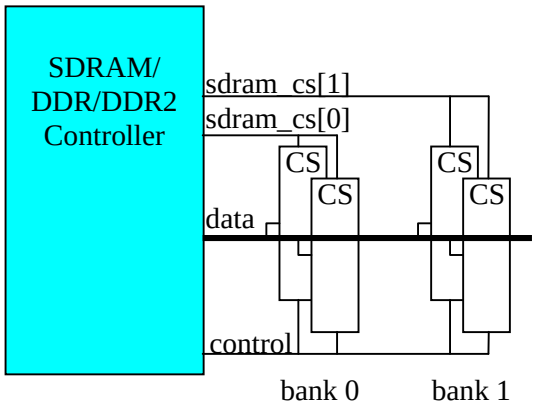
DDR2

- 3, 4, or 5 cycle CAS latency
- 4 or 8 SDRAM/DDR/DDR2 SDRAM internal banks
- 9, 10, 11, or 12 column address bits
- 13 or 14 row address bits

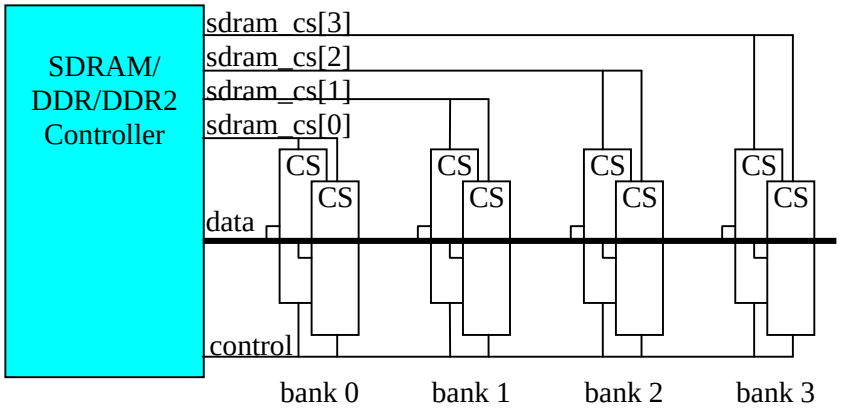
The SDRAM/DDR/DDR2 Controller supports one, two, or four SDRAM/DDR/DDR2 SDRAM banks (external banks) in SDRAM, DDR, and DDR2 SDRAM memory systems through its SDRAM/DDR/DDR2 Controller chip select outputs- sdram_cs[3:0]. The SDRAM/DDR/DDR2 SDRAM data bus, control lines, and clock are common to all banks of SDRAM/DDR/DDR2 SDRAM.



One SDRAM/DDR/DDR2 SDRAM Bank



Two SDRAM/DDR/DDR2 SDRAM Banks



Four SDRAM/DDR/DDR2 SDRAM Banks

The core is delivered as a synthesizeable RTL Verilog model. Deliverables include:

- RTL Verilog source code model of the core
- Verilog testbench and test cases
- Synthesis scripts examples
- Complete detailed documentation and training class notes