

## **AU-M2210: DDR/DDR2 Controller Core**

The AU-M2210 DDR/DDR2 Controller Core is a pipelined, high performance DDR and DDR2 SDRAM controller. Software configures the DDR/DDR2 Controller for either DDR or DDR2 SDRAM accesses. The DDR/DDR2 SDRAM data bus width is user configurable to 32 or 64 bits. The DDR/DDR2 Controller supports DDR and DDR2 SDRAM memory systems from 4 Mbytes to 4 Gbytes. DDR/DDR2 SDRAM timing parameters are software programmable to support a wide range of DDR and DDR2 SDRAM speed grades and clock frequencies. Refresh is initiated by the DDR/DDR2 Controller according to the software programmable refresh interval. To conserve power the DDR/DDR2 SDRAMs can be put in low power mode. The DDR/DDR2 Controller is available as a synthesizable Verilog model from Aurora VLSI, Inc. Contact [CustomerService@auroravlsi.com](mailto:CustomerService@auroravlsi.com).

The DDR/DDR2 Controller accepts DDR and DDR2 SDRAM requests and compares the request address to addresses of all active rows. If the request address falls in an active row, the request goes directly to the DDR/DDR2 SDRAMs without stalling the DDR/DDR2 Controller pipeline. This results in a peak bandwidth of 4 bytes/cycle with a 32 bit DDR/DDR2 SDRAM data bus, and 8 bytes/cycle with a 64 bit DDR/DDR2 SDRAM data bus. Once a row is activated, it is left activated so that the maximum amount of requests are to active rows, resulting in highest performance.

The number of row address bits, column address bits, bank address bits, and DDR/DDR2 SDRAM banks is software configurable. Nine to twelve column address bits are supported. The number of row address bits can be set to twelve, thirteen, or fourteen. DDR SDRAMs with four internal banks are supported. DDR2 SDRAMs with four or eight internal banks are supported. One, two, or four banks of DDR/DDR2 SDRAMs (external banks) can be built into the system. The DDR/DDR2 SDRAM chip select pins are used to identify the accessed bank of DDR/DDR2 SDRAM. This flexibility permits DDR/DDR2 SDRAM memory system of 4 Mbytes to 4 Gbytes.

DDR/DDR2 SDRAM timing parameters are software programmable. This allows the DDR/DDR2 Controller to be used with a wide range of DDR and DDR2 SDRAM speed grades and cycle times. CAS latency, DDR/DDR2 SDRAM drive strength, and ODT RTT (DDR2 only) are also software programmable.

The DDR/DDR2 SDRAM refresh interval is software programmable. Each time the refresh interval expires, the DDR/DDR2 Controller performs an auto-refresh cycle to all DDR/DDR2 SDRAM internal and external banks.

Upon reset, DDR and DDR2 SDRAM accesses are disabled. After programming the DDR/DDR2 Controller registers to configure the DDR/DDR2 SDRAM system- DDR or DDR2, sizes, timing parameters, CAS latency, etc., software enables DDR/DDR2 SDRAM accesses. Once enabled, the DDR/DDR2 Controller loads the DDR/DDR2 SDRAMs' Mode Registers, performs the appropriate refresh cycles, and is then ready to accept DDR/DDR2 SDRAM read and write requests.

The user may put the DDR/DDR2 SDRAMs into low power mode through software. The DDR/DDR2 Controller continues to initiate refresh cycles while the DDR/DDR2 SDRAMs are powered down. Low power mode is exited when a read/write request occurs or when software exits low power mode.

DDR/DDR2 Controller features are summarized:

- 32 bit or 64 bit DDR/DDR2 SDRAM data bus
- 4 Mbyte to 4 Gbyte DDR/DDR2 memory system
- Pipelined accesses to active rows for highest performance
- 1, 2, or 4 banks of DDR/DDR2 SDRAMs
- DDR/DDR2 SDRAM powerdown supported
- Fully programmable DDR/DDR2 SDRAM timing parameters
- Auto-refresh with programmable DDR/DDR2 SDRAM refresh interval

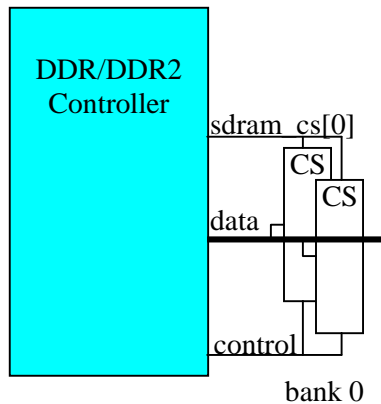
#### DDR

- 2, 2.5, or 3 cycle CAS latency
- 4 DDR SDRAM internal banks
- 9, 10, 11, or 12 column address bits
- 12, 13, or 14 row address bits

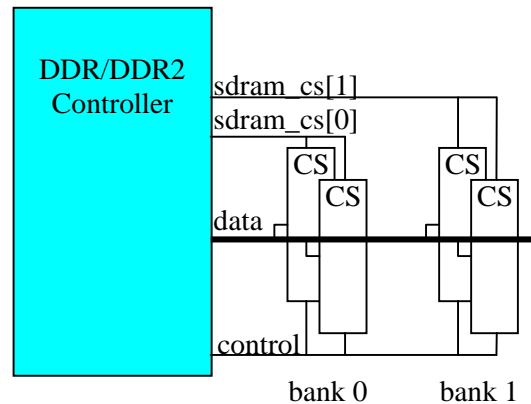
#### DDR2

- 3, 4, or 5 cycle CAS latency
- 4 or 8 DDR/DDR2 SDRAM internal banks
- 9, 10, 11, or 12 column address bits
- 13 or 14 row address bits

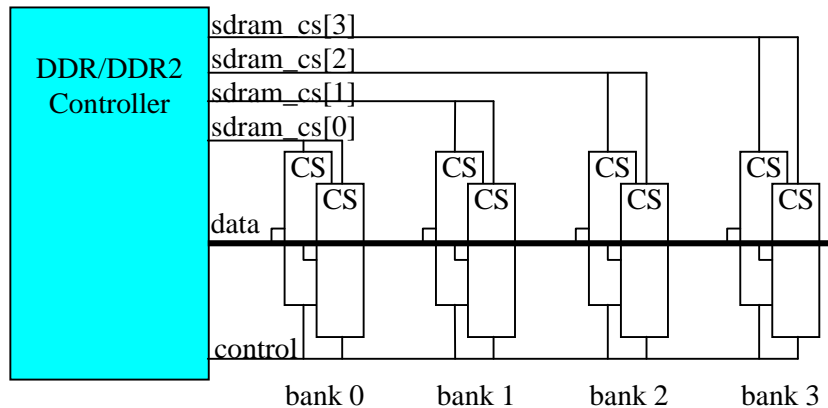
The DDR/DDR2 Controller supports one, two, or four DDR/DDR2 SDRAM banks (external banks) in DDR and DDR2 SDRAM memory systems through its DDR/DDR2 Controller chip select outputs- sdr<sub>am</sub>\_cs[3:0]. The DDR/DDR2 SDRAM data bus, control lines, and clock are common to all banks of DDR/DDR2 SDRAM.



One DDR/DDR2 SDRAM Bank



Two DDR/DDR2 SDRAM Banks



Four DDR/DDR2 SDRAM Banks

The core is delivered as a synthesizable RTL Verilog model. Deliverables include:

- RTL Verilog source code model of the core
- Verilog testbench and test cases
- Synthesis scripts examples
- Complete detailed documentation and training class notes