AU-M2010: DDR Controller Core

The AU-M2010 DDR Controller Core is a pipelined, high performance DDR SDRAM controller. The DDR SDRAM data bus width is user configurable to 32 or 64 bits. The DDR Controller supports DDR SDRAM memory systems from 4 Mbytes to 4 Gbytes. DDR SDRAM timing parameters are software programmable to support a wide range of DDR SDRAM speed grades and clock frequencies. Refresh is initiated by the DDR Controller according to the software programmable refresh interval. To conserve power the DDR SDRAMs can be put in low power mode. The DDR Controller is available as a synthesizable Verilog model from Aurora VLSI, Inc. Contact CustomerService@auroravlsi.com.

The DDR Controller accepts DDR SDRAM requests and compares the request address to addresses of all active rows. If the request address falls in an active row, the request goes directly to the DDR SDRAMs without stalling the DDR Controller pipeline. This results in a peak bandwidth of 4 bytes/cycle with a 32 bit DDR SDRAM data bus, and 8 bytes/cycle with a 64 bit DDR SDRAM data bus. Once a row is activated, it is left activated so that the maximum amount of requests are to active rows, resulting in highest performance.

The number of row address bits, column address bits, and DDR SDRAM banks is software configurable. Nine to twelve column address bits are supported. The number of row address bits can be set to twelve, thirteen, or fourteen. DDR SDRAMs with four internal banks are supported. One, two, or four banks of DDR SDAMs (external banks) can be built into the system. The DDR SDRAM chip select pins are used to identify the accessed bank of DDR SDRAM. This flexibility permits DDR SDRAM memory system of 4 Mbytes to 4 Gbytes.

DDR SDRAM timing parameters are software programmable. This allows the DDR Controller to be used with a wide range of DDR SDRAM speed grades and cycle times. CAS latency and DDR SDRAM drive strength are also software programmable.

The DDR SDRAM refresh interval is software programmable. Each time the refresh interval expires, the DDR Controller performs an auto-refresh cycle to all DDR SDRAM internal and external banks.

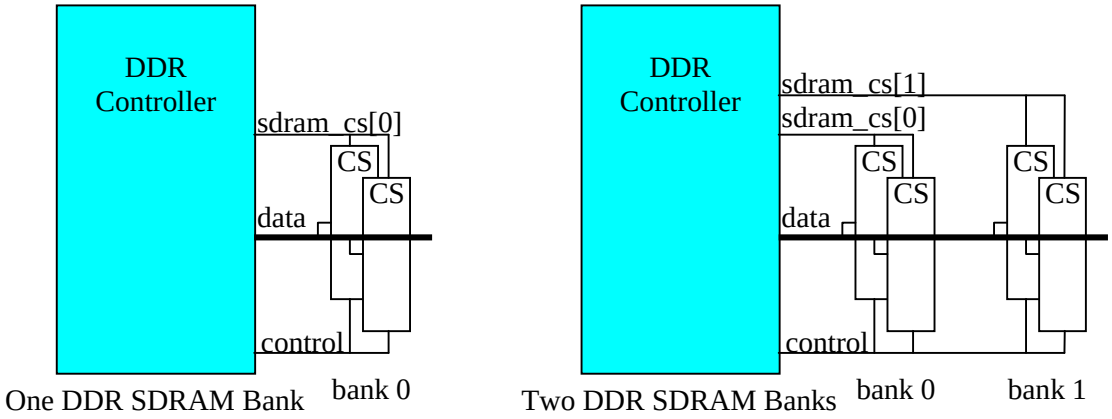
Upon reset, DDR SDRAM accesses are disabled. After programming the DDR Controller registers to configure the DDR SDRAM system- sizes, timing parameters, CAS latency, etc., software enables DDR SDRAM accesses. Once enabled, the DDR Controller loads the DDR SDRAMs' Mode Registers, performs the appropriate refresh cycles, and is then ready to accept DDR SDRAM read and write requests.

The user may put the DDR SDRAMs into low power mode through software. The DDR Controller continues to initiate refresh cycles while the DDR SDRAMs are powered down. Low power mode is exited when a read/write request occurs or when software exits low power mode.

DDR Controller features are summarized:

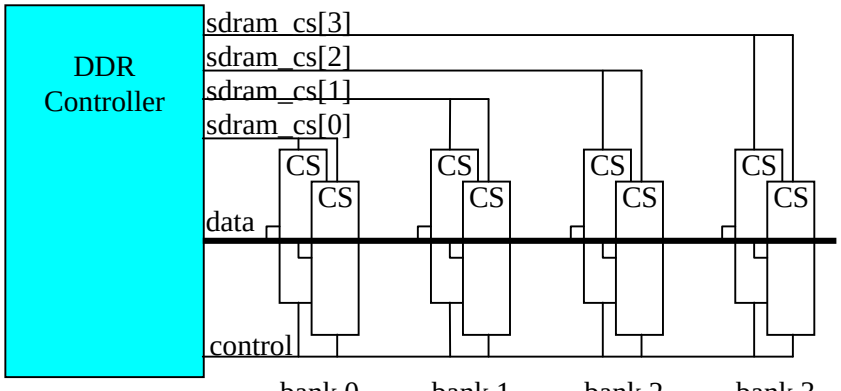
- 32 bit or 64 bit DDR SDRAM data bus
- 4 Mbyte to 4 Gbyte DDR memory system
- Pipelined accesses to active rows for highest performance
- 2, 2.5, or 3 cycle CAS latency
- 1, 2, or 4 banks of DDR SDRAMs
- 4 DDR SDRAM internal banks
- 9, 10, 11, or 12 column address bits
- 12, 13, or 14 row address bits
- DDR SDRAM powerdown supported
- Fully programmable DDR SDRAM timing parameters
- Auto-refresh with programmable DDR SDRAM refresh interval

The DDR Controller supports one, two, or four DDR SDRAM banks (external banks) in DDR SDRAM memory systems through its DDR Controller chip select outputs- sdram_cs[3:0]. The DDR SDRAM data bus, control lines, and clock are common to all banks of DDR SDRAM.



One DDR SDRAM Bank

Two DDR SDRAM Banks



Four DDR SDRAM Banks

The core is delivered as a synthesizeable RTL Verilog model. Deliverables include:

- RTL Verilog source code model of the core
- Verilog testbench and test cases
- Synthesis scripts examples
- Complete detailed documentation and training class notes