AU-M2000: SDRAM Controller Core

The AU-M2000 SDRAM Controller Core is a pipelined, high performance SDRAM controller. The SDRAM data bus width is user configurable to 32 or 64 bits. The SDRAM Controller supports SDRAM memory systems from 4 Mbytes to 4 Gbytes. SDRAM timing parameters are software programmable to support a wide range of SDRAM speed grades and clock frequencies. Refresh is initiated by the SDRAM Controller according to the software programmable refresh interval. To conserve power the SDRAMs can be put in low power mode. The SDRAM Controller is available as a synthesizable Verilog model from Aurora VLSI, Inc. Contact CustomerService@auroravlsi.com.

The SDRAM Controller accepts SDRAM requests and compares the request address to addresses of all active rows. If the request address falls in an active row, the request goes directly to the SDRAMs without stalling the SDRAM Controller pipeline. This results in a peak bandwidth of 4 bytes/cycle with a 32 bit SDRAM data bus, and 8 bytes/cycle with a 64 bit SDRAM data bus. Once a row is activated, it is left activated so that the maximum amount of requests are to active rows, resulting in highest performance.

The number of row address bits, column address bits, bank address bits, and the SDRAM banks is software configurable. Eight to twelve column address bits are supported. The number of row address bits can be set to eleven, twelve, or thirteen. SDRAMs with either two or four internal banks are supported. One, two, or four banks of SDRAM (external banks) can be built into the system. The SDRAM chip select pins are used to identify the accessed bank of SDRAM. This flexibility permits SDRAM memory system of 4 Mbytes to 4 Gbytes.

SDRAM timing parameters are software programmable. This allows the SDRAM Controller to be used with a wide range of SDRAM speed grades and cycle times. CAS latency is also software programmable.

The SDRAM refresh interval is software programmable. Each time the refresh interval expires, the SDRAM Controller performs an auto-refresh cycle to all SDRAM internal and external banks.

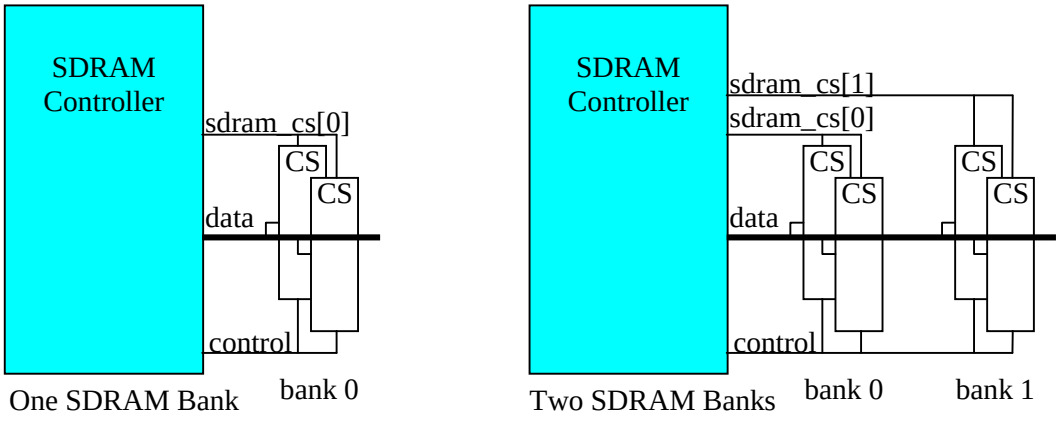
Upon reset, SDRAM accesses are disabled. After programming the SDRAM Controller registers to configure the SDRAM system- sizes, timing parameters, CAS latency, etc., software enables SDRAM accesses. Once enabled, the SDRAM Controller loads the SDRAMs' Mode Registers, performs the appropriate refresh cycles, and is then ready to accept SDRAM read and write requests.

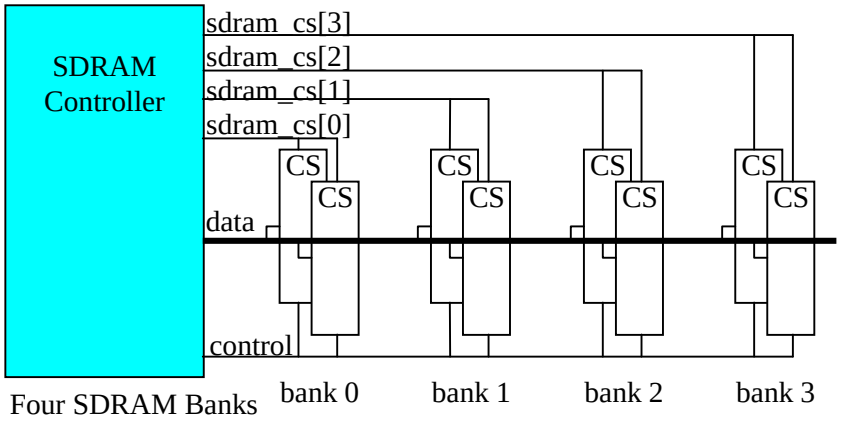
The user may put the SDRAMs into low power mode through software. The SDRAM Controller continues to initiate refresh cycles while the SDRAMs are powered down. Low power mode is exited when a read/write request occurs or when software exits low power mode.

SDRAM Controller features are summarized:

- 32 bit or 64 bit SDRAM data bus
- 4 Mbyte to 4 Gbyte SDRAM memory system
- Pipelined accesses to active rows for highest performance
- 2 or 3 cycle CAS latency
- 1, 2, or 4 banks of SDRAM
- 2 or 4 SDRAM internal banks
- 8, 9, 10, 11, or 12 column address bits
- 11, 12, or 13 row address bits
- SDRAM powerdown supported
- Fully programmable SDRAM timing parameters
- Auto-refresh with programmable SDRAM refresh interval

The SDRAM Controller supports one, two, or four SDRAM banks (external banks) in SDRAM memory systems through its SDRAM chip select outputs- sdram_cs[3:0]. The SDRAM data bus, control lines, and clock are common to all banks of SDRAM.





The core is delivered as a synthesizeable RTL Verilog model. Deliverables include:

- RTL Verilog source code model of the core
- Verilog testbench and test cases
- Synthesis scripts examples
- Complete detailed documentation and training class notes