AU-M1000: SRAM Controller Core

The AU-M1000 SRAM Controller Core is a versatile, pipelined, high performance SRAM controller. Several SRAM types are supported including flow through ZBT synchronous SRAMs, pipelined ZBT synchronous SRAMs, flow through syncburst synchronous SRAMs, SCD syncburst synchronous SRAMs, DCD syncburst synchronous SRAMs, and asynchronous SRAMs. The SRAM Controller supports SRAM memory systems from 512 Kbytes to 512 Mbytes. The SRAM data bus width is user configurable to 32 or 64 bits. To conserve power the SRAMs can be put in low power mode. The SRAM Controller is available as a synthesizable Verilog model from Aurora VLSI, Inc. Contact CustomerService@auroravlsi.com.

The SRAM Controller accepts SRAM requests and converts them into pipelined SRAM accesses within the SRAM Controller. This results in a peak bandwidth of 4 bytes/cycle with a 32 bit SRAM data bus, and 8 bytes/cycle with a 64 bit SRAM data bus. The SRAM Controller ensures that correct latencies and bus turn around times are met.

The number of SRAM address bits and SRAM banks is software configurable. Seventeen to twenty four address bits are supported. One, two, or four banks of SRAM can be built into the system. The SRAM chip select pins are used to identify the accessed bank of SRAM. This flexibility permits SRAM memory system of 512 Kbytes to 512 Mbytes.

SRAM read and write latencies are software programmable. This allows the SRAM Controller to be used with a wide variety of SRAMs. Asynchronous SRAMs and many types of synchronous SRAMs are supported.

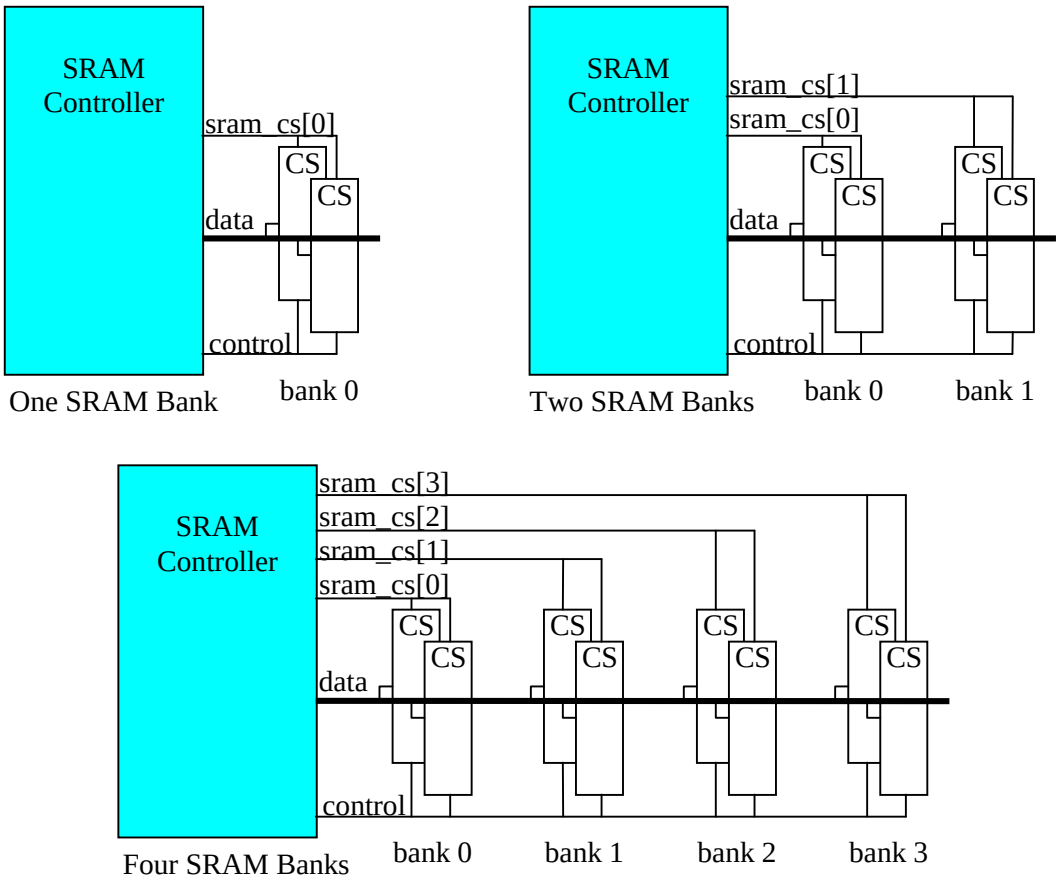
Upon reset, SRAM accesses are optionally enabled or disabled according to a user configurable Verilog parameter. Software may also enable and disable SRAM accesses. Read and write latencies, the number of address bits, and number of SRAM banks are also user configurable upon reset with Verilog parameters. After reset de-assertion, software may overwrite the read and write latencies, number of address bits, and number of SRAM bank reset values.

The user may put the SRAMs into low power mode through software. Low power mode is exited when a read/write request occurs or when software exits low power mode.

SRAM Controller features are summarized:

- Supports several SRAM types- flow through ZBT synchronous, pipelined ZBT synchronous, flow through syncburst synchronous, SCD syncburst synchronous, DCD syncburst synchronous, and asynchronous SRAMs
- 32 bit or 64 bit SRAM data bus
- 512 Kbyte to 512 Mbyte SRAM memory system
- Pipelined accesses for highest performance
- 0, 1, or 2 cycle read latency
- 0, 1, or 2 cycle write latency
- 1, 2, or 4 banks of SRAM
- 17 to 24 address bits
- SRAM powerdown supported

The SRAM Controller supports one, two, or four SRAM banks in SRAM memory systems through its SRAM chip select outputs- sram_cs[3:0]. The SRAM data bus, control lines, and clock are common to all banks of SRAM.



The core is delivered as a synthesizeable RTL Verilog model. Deliverables include:

- RTL Verilog source code model of the core
- Verilog testbench and test cases
- Synthesis scripts examples
- Complete detailed documentation and training class notes