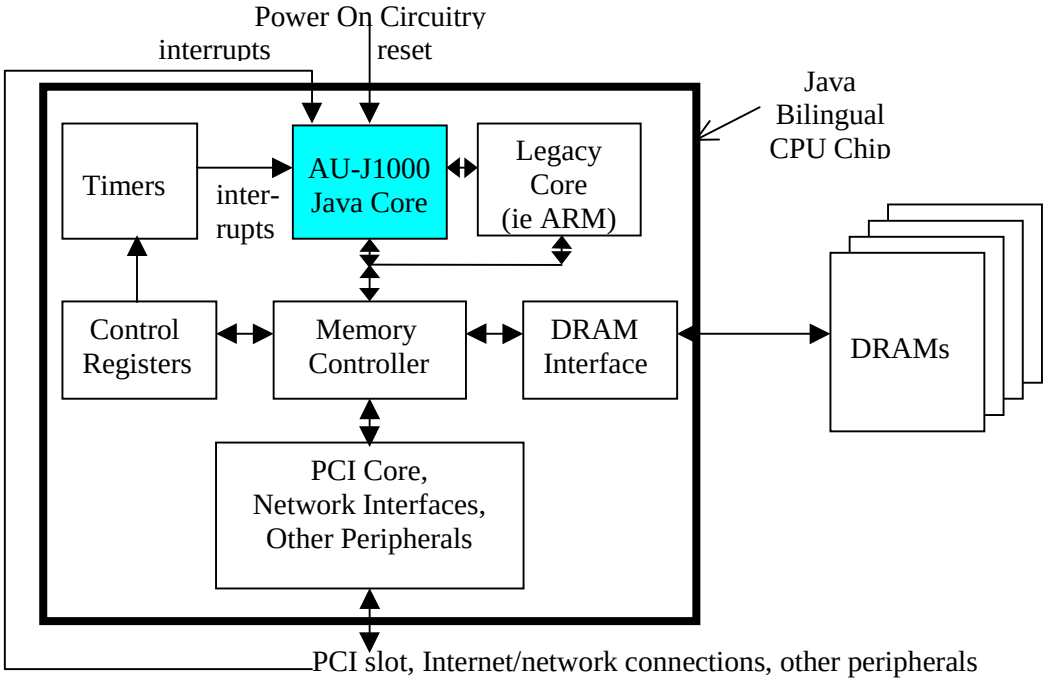
# AU-J1000: High Performance Java Processor Core

The AU-J1000 Java Processor Core is a Java processor core targeted at efficient high performance Java execution. With a CaffeineMarks overall score of 20 CaffeineMarks/MHz, Java performance is significantly faster than other software *and* hardware Java solutions. This is due to several proprietary mechanisms that boost Java performance. For software compatibility, the Java Core can be integrated with a legacy core (such as Power PC, x86, ARM, etc.). Power management hardware ensures that only the active core consumes power at any given time. The AU-J1000 Java Processor Core is available as a synthesizable Verilog model from Aurora VLSI, Inc. Contact CustomerService@auroravlsi.com. Aurora VLSI can also integrate it with a legacy core upon customer request.

The AU-J1000 Java Core is intended for a wide variety of high end Java applications. It can be integrated into numerous types of chips that run Java. A few possibilities include:

- Java host CPU chips used as the central processor in
  - Cell phones, Smart phones
  - Internet appliances
  - Home gateways and servers
  - Set top boxes, DTVs, personal TVs
  - Game stations
  - Smart card servers
  - Enterprise Java acceleration
- High performance dual processor chips with an integrated Java coprocessor as one of the two processors



The AU-J1000 Java Core is a single scalar processor core targeted at efficient, high performance Java execution. Several proprietary techniques that address Java specific architectural features, result in high speed Java execution. The AU-J1000 Java Core runs all Java bytecodes defined in "The Java Virtual Machine Specification".

The AU-J1000 Java Core achieves its high performance with a single scalar architecture that utilizes a five stage pipeline. Integer and floating point operation units are included. This pipeline and these operation units provide resources that allow multiple bytecodes to execute each cycle.

The Java Core includes an instruction cache and a data cache. The sizes of these caches are configurable from 32 bytes to 8K bytes. Interrupt logic allows external events/logic to interrupt the Java Core. Proprietary bytecodes are implemented for system functions, and so that the Java Virtual Machine can run on the Java Core.

The Java Core interfaces to external logic through two high bandwidth cache ports and an interrupt interface. Both the instruction cache and data cache have 64 bit interfaces to external memory logic. At 200 MHz, this provides a bandwidth of 1.6 Gbytes/sec into both the instruction and data caches, for a total bandwidth of 3.2 Gbytes/sec into the Java Core. These high bandwidth cache ports help ensure high performance. The interrupt interface includes sixteen independent interrupt request lines and an interrupt acknowledge.

A bus interface and memory interface for the AU-J1000 Processor Core is provided by the AU-S1000 Processor Memory and Bus Interface Core or AU-SB1000 Processor Memory and AMBA AHB Bus Interface Core from Aurora VLSI. These Memory and Bus Interface Cores connect seamlessly to the AU-J1000 Processor Core.

AU-J1000 Java Core features are summarized:

- Hardware accelerated Java execution- 20 CaffeineMarks/MHz (measured)
- Proprietary hardware accelerates common Java specific functions
- Execution of all "The Java Virtual Machine Specification" bytecodes
- Proprietary bytecode execution for the JVM run time system (system functions)
- 5 stage RISC pipeline
- Configurable instruction cache- 32 to 8K bytecodes
- Configurable data cache- 32 to 8K bytes
- Interrupts- 16 interrupt request lines and software interrupts
- High bandwidth memory interface
- Seamless connection to Processor Memory and Bus Interface Cores from Aurora VLSI that provide a bus interface and memory interface

The core is delivered as a synthesizeable RTL Verilog model. Deliverables include:

- RTL Verilog source code model of the core
- Verilog testbench and test cases
- Synthesis scripts examples
- Complete detailed documentation and training class notes