AU-G0700: Reset Controller AMBA APB Core

The AU-G0700 Reset Controller AMBA APB Core provides a reset controller peripheral for AMBA based SOCs. It aggregates two pin resets, two interrupt/watchdog resets, and software reset capabilities into 32 individual reset signals for use throughout an SOC. It connects seamlessly to the AMBA APB Bus as an AMBA Bus slave. The Reset Controller AMBA APB Core is available as a synthesizable Verilog model from Aurora VLSI, Inc. Contact CustomerService@auroravlsi.com.

The Reset Controller generates up to 32 reset outputs from two pin resets, two interrupt/watchdog resets, and software reset requests. Each reset output stays asserted for a user configurable reset de-assertion delay time, after the reset request is de-asserted. This reset de-assertion delay time is independently configured for each reset output. The maximum reset de-assertion delay is 64K cycles. Each reset output is independently configured for active high or active low reset signaling.

Two nonmaskable pin reset requests are provided. They can be configured as active high or active low reset requests. Each reset output is asserted asynchronously and de-asserted synchronously when a pin reset occurs.

Two interrupt/watchdog reset requests are provided. They can be configured as active high or active low reset requests. These reset requests are independently enabled for each reset output. Each reset output that is enabled for an interrupt/watchdog reset request, is synchronously asserted and de-asserted when that interrupt/watchdog reset request occurs.

Software can independently set each of the 32 reset outputs. Reset output assertion and de-assertion is synchronous for software reset. Optionally for each reset output, software reset can be automatically cleared after the reset de-assertion delay time.

The Reset Controller AMBA APB Core features are summarized:

- Up to 32 reset outputs (configurable)- asserted high or low (configurable)
- Configurable reset de-assertion delay up to 64K cycles for each reset output
- 2 pin reset requests
  - nonmaskable
  - asynchronously asserted, synchronously de-asserted
  - asserted high or low (configurable)
- 2 interrupt/watchdog reset requests
  - individually maskable for each reset output
  - synchronously asserted, synchronously de-asserted
  - asserted high or low (configurable)
- Software reset requests
  - individually asserted by software for each reset output
  - synchronously asserted, synchronously de-asserted

The core is delivered as a synthesizeable RTL Verilog model. Deliverables include:

- RTL Verilog source code model of the core
- Verilog testbench and test cases
- Synthesis scripts examples
- Complete detailed documentation and training class notes