AU-G0500: General Purpose I/Os AMBA APB Core

The AU-G0500 General Purpose I/Os (GPIOs) AMBA APB Core provides a GPIO peripheral for AMBA based SOCs. It contains 32 General Purpose I/Os (GPIOs) that connect seamlessly to the AMBA APB Bus as an AMBA Bus slave. The General Purpose I/Os AMBA APB Core is available as a synthesizable Verilog model from Aurora VLSI, Inc. Contact CustomerService@auroravlsi.com.

32 general purpose I/Os (GPIOs) that connect directly to chip pins, are provided. Each GPIO is software configured over the AMBA bus to operate in either register mode or bypass mode. In register mode software also configures each GPIO as either an input or output. In bypass mode, the directionality of each GPIO is determined by the data enable input to the GPIO Core.

As an output, in register mode, the output data is written to the GPIO Core over the AMBA Bus. Each output bit can also be set or cleared from the AMBA bus in register mode. In bypass mode, the output data is driven directly to the pins from the data bypass input to the GPIO Core.

Input data from the pins is captured in the GPIO Core for each GPIO. In register mode, this input data is read over the AMBA Bus. In bypass mode, the input data is available through the GPIO Core, directly from the pin at the GPIO Core data bypass output.

Each GPIO can be used to signal an interrupt. These GPIO interrupts are enabled independently for each GPIO. Level or edge sensitivity, and interrupt input polarity are configured independently for each GPIO by software. GPIO inputs are deglitched for interrupt detection.

The General Purpose I/Os AMBA APB Core features are summarized:

- 32 GPIOS
- Register or bypass mode selected independently for each GPIO
- Independent direction control for each GPIO
- Output data can be
  - programmed, set, or cleared over the AMBA bus (register mode)
  - driven directly to the output pins (bypass mode)
- Output enable can be
  - programmed over the AMBA bus (register mode)
  - driven directly to the output pins (bypass mode)
- Output enable assertion polarity is user configurable
- Input data can be
  - captured and read over the AMBA bus (register mode)
  - directly available from the input pins (bypass mode)
- Independent interrupt enable for each GPIO
- GPIO inputs are deglitched for interrupt detection
- Level or edged sensitive interrupts- independently configured for each interrupt
- High or low interrupt polarity- independently configured for each interrupt

The core is delivered as a synthesizeable RTL Verilog model. Deliverables include:

- RTL Verilog source code model of the core
- Verilog testbench and test cases
- Synthesis scripts examples
- Complete detailed documentation and training class notes