AU-G0100: Interrupt Controller AMBA APB Core

The AU-G0100 Interrupt Controller AMBA APB Core provides an interrupt controller peripheral for AMBA based SOCs. It aggregates 32 interrupt requests into 8 interrupt outputs. It connects seamlessly to the AMBA APB Bus as an AMBA Bus slave. The Interrupt Controller AMBA APB Core is available as a synthesizable Verilog model from Aurora VLSI, Inc. Contact CustomerService@auroravlsi.com.

The Interrupt Controller captures interrupt requests from 32 interrupt inputs. Each interrupt input is independently configured for level or edge sensitive interrupt requests, and for active high or active low interrupt requests. The interrupt inputs are deglitched.

The 32 interrupt inputs are individually enabled by software. Each interrupt request at an enabled interrupt input becomes a pending interrupt. Each pending interrupt can cause an interrupt to be signaled at one or more of the interrupt outputs. Software configures the Interrupt Controller to indicate the interrupt inputs that trigger each interrupt output.

Each interrupt input is assigned a priority level, from 0 to 31, by software. The highest priority level is configurable to be either 0 or 31. When an interrupt occurs at one of the eight interrupt outputs, the priority level of the highest priority interrupt request that contributed to assertion of that interrupt output, is available to be used for vectored interrupt handling. Each interrupt output also has a pending register that shows all of its pending interrupts, and a service register that shows all of its highest priority pending interrupts.

Each of the 32 possible interrupt requests can be set by software. Pending interrupts are cleared by software.

The Interrupt Controller AMBA APB Core features are summarized:

- 32 interrupt requests
  - independently enabled
  - level or edge sensitive (configurable)
  - active high or low (configurable)
  - deglitched
- 8 interrupt outputs (configurable)
- Each interrupt request is assigned to one or more interrupt outputs that it will trigger
- 32 interrupt request priority levels
- Each interrupt request is assigned a priority level
- Priority level of highest priority interrupt request for each interrupt output is available for vectored interrupt handling
- Pending registers show all pending interrupt requests
- Service registers show highest priority pending requests
- Software interrupt set and clear

The core is delivered as a synthesizeable RTL Verilog model. Deliverables include:

- RTL Verilog source code model of the core
- Verilog testbench and test cases
- Synthesis scripts examples
- Complete detailed documentation and training class notes