Aurora VLSI

Unleashing the Power of the Internet

AU-C02XX: 32 Bit, Tiny, Low Power SPARC Processor Cores

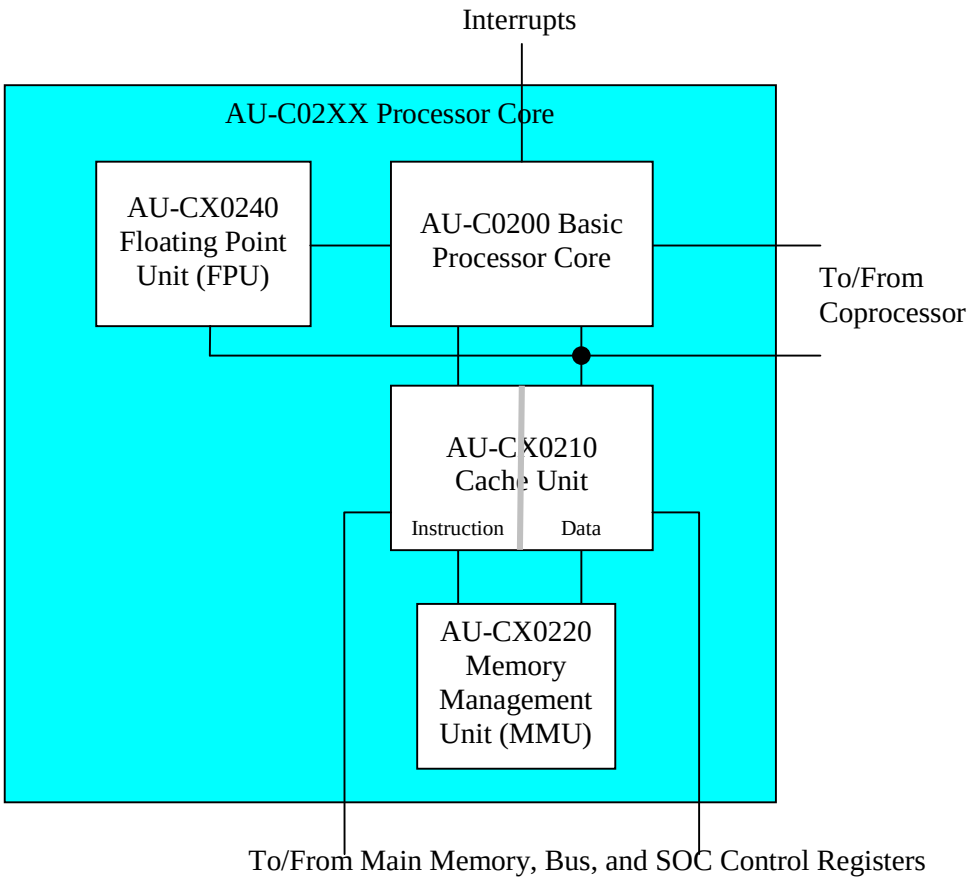
The AU-C02XX 32 Bit Tiny, Low Power SPARC Processor Cores are a family of small, low power 32 bit SPARC processor cores targeted at embedded controller, wireless, and other portable applications. For lowest power and smallest gate count, each processor of this family of processor cores, includes the base processor and a combination of any of a) caches, b) MMU, and/or c) floating point. The user selects the processor from this processor family that has only user's required functionality, and therefore does not waste area or power on unnecessary functions. Power consumption is expected to be .3mW/MHz or less in .18u technologies. Power levels in the .15mW/MHz range can be attained with cell libraries that support lower supply voltages (1.2V). The AU-C02XX Processor Cores are available as synthesizable Verilog models from Aurora VLSI, Inc. Contact CustomerService@auroravlsi.com.

The AU-C02XX Processor Cores are ideal for embedded applications that have outgrown 16 bit controllers and therefore want to move up to a 32 bit controller. Their low gate counts and power dissipation make them attractive to a wide variety of wireless and portable applications. They can be integrated into numerous types of chips for embedded systems and battery based systems. A few possibilities include:

- Wireless Internet appliances- email, browsers, Web phones
- Cell phones
- PDAs, handheld computers, electronic organizers
- Digital cameras- still and video
- Smart appliances
- Automotive applications

The AU-C02XX Processor Cores have a modular system architecture as shown in the figure below. In addition to the basic processor, there are modules for the caches, virtual memory, and floating point- the AU-CX0210 Cache Unit, AU-CX0220 MMU Unit, and AU-CX0240 Floating Point Unit. Therefore, although caches, an MMU, and floating point are not included in the basic AU-C0200 Processor Core, if caches, virtual addressing, and/or floating point are desired, the AU-CX0210 Cache Unit, AU-CX0220 MMU Unit, and/or the AU-CX0240 Floating Point Unit can be attached to the basic AU-C0200 Processor Core for the desired functionality. The table below shows all possible combinations that make up the AU-C02XX Processor Core family. This provides a flexible system architecture where users can minimize gate count and power dissipation by only including the modules necessary for their applications.

AU-C02XX Processor Core	Description
AU-C0200	Basic processor only
AU-C0210	Basic processor + caches
AU-C0230	Basic processor + caches + MMU
AU-C0240	Basic processor + floating point
AU-C0250	Basic processor + caches + floating point
AU-C0270	Basic processor + caches + MMU + floating point



The AU-C02XX Processor Cores interface to external logic through two high bandwidth memory ports, a coprocessor port for the optional user defined coprocessor, and an interrupt interface. Both the instruction fetches and data accesses each have 32 bit interfaces to external memory logic. At 250 MHz, this provides a bandwidth of 1 Gbytes/sec for both instruction and data transfers to/from the core, for a total bandwidth of 2 Gbytes/sec into the AU-C02XX Processor Cores. These high bandwidth memory ports help ensure high performance. The coprocessor port provides facilities for instruction transfer to the coprocessor, flow control, coprocessor loads and stores, register data movement to/from the coprocessor, and coprocessor condition codes for the coprocessor branches. The interrupt interface includes sixteen independent interrupt request lines that are always monitored.

A bus interface and memory interface for the AU-C02XX Processor Core family is provided by the AU-S1000 Processor Memory and Bus Interface Core or AU-SB1000 Processor Memory and AMBA AHB Bus Interface Core from Aurora VLSI. These Memory and Bus Interface Cores connect seamlessly to any AU-C02XX Processor Core.

AU-C02XX Processor Core features are summarized:

- Low gate count
- Low power
- High clock rate- 200/350MHz in worst case slow/typical .18u conditions
- Modular architecture- Basic Processor Core, Cache Unit, MMU, FPU
- Seamless connection to Processor Memory and Bus Interface Cores from Aurora VLSI that provide a bus interface and memory interface

Basic Processor Core

- Smallest possible 32 bit processor core
- 20K – 25K gates
- Low power- .15 - .3mW/MHz
- 32 bit SPARC instruction set
- Good performance- 160/280 Dhrystone 2.1 at 200/350MHz (predicted)
- Peak execution rate of 1 instruction/cycle (single scalar design)
- 5 stage RISC pipeline
- Coprocessor port for an optional user defined coprocessor
- Interrupt interface

Cache Unit

- Separate instruction and data cache
- Sizes are configurable from 256 bytes to 8Kbytes each
- Direct mapped
- 16 byte line sizes
- Writeback data cache
- Physically addressed (virtually indexed when MMU Unit is present)
- Byte parity
- Direct access to data and tags of each cache for cache management
- Separate instruction and data high bandwidth memory interfaces- 4 bytes/cycle peak

Memory Management Unit (MMU)

- SPARC reference MMU
- Simultaneous instruction and data virtual address translation for high performance
- 4K byte page size
- TLB
  - 32 or 64 entries (configurable)
  - Dual ported
  - Hardware replacement upon TLB miss

Floating Point Unit (FPU)

- IEEE754-1985 floating point
- Fully compliant results for all floating point instructions computed in hardware
- Single and double precision
- Supports 32 bit and 64 bit floating point data loads and stores
- Floating point condition codes for floating point conditional branches

The core is delivered as a synthesizeable RTL Verilog model. Deliverables include:

- RTL Verilog source code model of the core
- Verilog testbench and test cases
- Synthesis scripts examples
- Complete detailed documentation and training class notes

Basic Processor Core

The AU-C02XX Processor Cores are 32 bit SPARC processor cores. An AU-C02XX Processor is an efficient single scalar 32 bit processor based on a five stage RISC pipeline. Due to its efficient design, clock rates up to 350MHz (typical conditions) are predicted with standard ASIC implementations in .18u technology. Its peak execution rate is one instruction/cycle. Predicted Dhrystone 2.1 performance is 160/280 at 200/350MHz.

A coprocessor port is provided so that the user can optionally expand the processor functionality by defining and attaching a coprocessor that provides additional functions that are important to the user's application.

Interrupt logic allows external events/logic to interrupt the AU-C02XX Processor Cores.

Cache Unit

The Cache Unit provides caches for the AU-C02XX Processor Cores. It consists of an instruction cache and a data cache. The size of each cache can be separately configured from 256 bytes to 8Kbytes. These caches are direct mapped with line sizes of 16 bytes. The data cache is a writeback cache. The caches are physically addressed. When the Memory Management Unit is included, the caches are virtually indexed. Cache data and tags are protected by byte parity.

For high performance, each cache has a high bandwidth, dedicated interface to the Basic Processor Core, and a high bandwidth, dedicated interface to the memory system. These interfaces run at the Basic Processor Core clock rate. They have separate 32 bit data and address buses. At 250 MHz, this provides a bandwidth of 1 Gbyte/sec for both instruction and data transfers to/from the Processor Core, for a total bandwidth of 2 Gbytes/sec into the Processor Core. The bandwidth to the memory system is also 1Gbyte/sec for each interface to memory. Thus, the total bandwidth to the memory system is also 2Gbytes/sec.

The Cache Unit size is contingent on the choice of cache sizes. It ranges from 3K gates to 86K gates as shown in the table below.

Cache Sizes	Cache Unit Gate Count
256 byte instruction and data caches	3K
512 byte instruction and data caches	6K
1 Kbyte instruction and data caches	11K
2 Kbyte instruction and data caches	22K
4 Kbyte instruction and data caches	43K
8 Kbyte instruction and data caches	86K

Gate Count vs. Cache Size

Memory Management Unit (MMU)

The Memory Management Unit (MMU) provides virtual address translation for the Basic Processor Core. 32 bit virtual addresses are translated to 32 bit physical addresses by the MMU. Address translation is done in parallel with instruction and data cache lookup resulting in single cycle cache accesses when a hit occurs in both the cache and MMU. The page size is 4K bytes.

The MMU contains a two port TLB and can therefore, simultaneously translate instruction and data virtual addresses. The TLB size can be configured to 32 or 64 entries. Upon a TLB miss, TLB entries are replaced by hardware.

The MMU has separate instruction and data interfaces to both the Basic Processor Core and Cache Unit. These separate interfaces allow simultaneous translation of instruction and data addresses, resulting in highest performance. The MMU accepts translation requests with their virtual addresses, from the Cache Unit. It then returns the physical address to the Cache Unit, in the next cycle.

Floating Point Unit (FPU)

The Floating Point Unit (FPU) provides IEEE754-1985 compliant single and double precision floating point for the Basic Processor Core. IEEE754-1985 compliant results are completely computed by hardware.

The FPU implements all four IEEE rounding modes- round to nearest, round to zero, round to positive infinity, and round to negative infinity. All five IEEE floating point traps are detected- invalid operation, underflow, overflow, inexact, and divide by zero.

For highest performance, the FPU is pipelined and runs at the Basic Processor Core clock rate. Floating point data is transferred directly from/to the data cache by the floating point load and store instructions.