AU-B3000: AMBA AHB Bus Master Core

The AU-B3000 AMBA AHB Bus Master provides the bus master function for the AMBA AHB Bus. It accepts requests from the user's logic and turns them into AMBA Bus transactions on the AMBA AHB Bus. The AMBA AHB Bus Master is available as a synthesizable Verilog model from Aurora VLSI, Inc. Contact CustomerService@auroravlsi.com.

The AMBA Master can interface to either a 32 bit or 64 bit AMBA AHB Bus. A Verilog parameter indicates the AMBA Bus width for the AMBA Master.

The AMBA Master is fully pipelined for highest throughput, and therefore highest system performance. It can issue AMBA Bus requests, drive AMBA Bus data, and capture data from the AMBA Bus, each AMBA Bus clock cycle.

The AMBA Master supports all required AMBA AHB Bus features including all AMBA burst and wrapping types, AMBA sizes up to the AMBA Bus width, and the AMBA Bus lock feature. Request lengths of up to 32 Kbytes from the user are supported and translated into one or more AMBA Bus transactions. When an AMBA slave responds with the RETRY or SPLIT response, the AMBA Master responds accordingly to eventually complete the transaction. This is transparent to the user (accept for the additional delay).

The user issues AMBA Bus requests to the AMBA Master according to a simple request/acknowledge protocol at the AMBA Master/Requester interface. After accepting a request, the AMBA Master initiates and completes an AMBA Bus transaction for the accepted request. The AMBA Master interfaces directly onto the AMBA bus and takes care of all AMBA Bus protocol requirements for the transaction. If the transaction is a read transaction, the AMBA Master assembles the read data from the AMBA Bus and returns it to the requester using a simple valid/ready protocol at the AMBA Master/Requester interface

Write data transmission on the AMBA Bus may be ended early by the user if necessary. For example, if the user's logic finds bad write data before the last write data of a write request, it may end the write transaction on the AMBA bus early by asserting the write abort signal at the AMBA Master/Requester interface.

The AMBA Master returns read errors from the AMBA Bus to the user. The read error from a slave's ERROR response, is returned to the user along with the read data that came with the slave's ERROR response. The user interprets the read data that came with the read error according to the slave's definition of read data with the ERROR response. Slave ERROR responses upon AMBA Bus writes are not returned to the user. Writes fail silently.

Data to/from the requester can be either big endian or little endian. The AMBA Master Control Register indicates the endianness.

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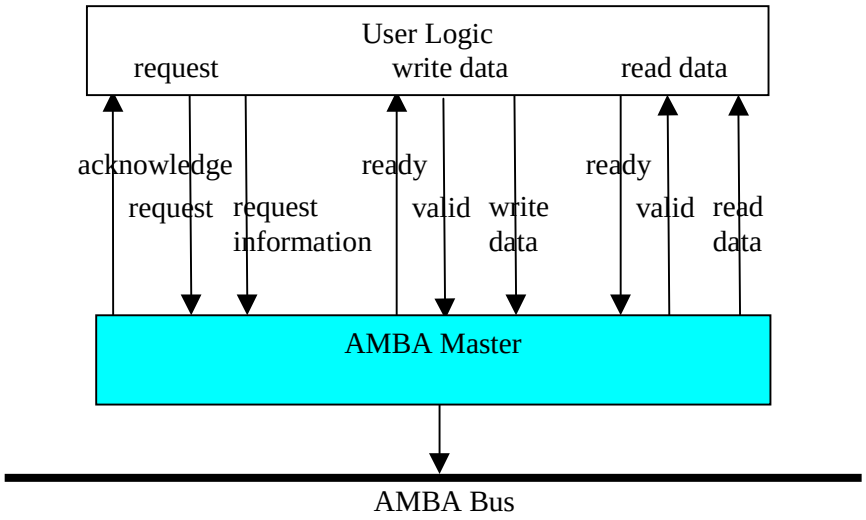
AMBA Bus Master features are summarized:

- AMBA AHB Bus master function
- 32 bit or 64 bit AMBA AHB Bus- user configurable
- Fully pipelined for highest throughput
- Supports all required AMBA AHB Bus features
- Simple request/acknowledge and valid/ready requester interface protocols
- Write abort to terminate writes early
- AMBA Bus read error returned to the user with the read data
- Big endian and little endian modes

The AMBA Master is used to interface user logic that must initiate AMBA AHB Bus transactions, to the AMBA Bus. This is shown below.



The user's logic issues requests to the AMBA Master along with the request information. The request and request information is driven continuously until the AMBA Master acknowledges the request.

To transfer write data to the AMBA Master, the user asserts the write data valid signal and drives the write data until the AMBA Master accepts the write data. The AMBA Master indicates that it is accepting write data by asserting the write data ready signal in the cycle when it accepts the write data.

To return read data to the requester, the AMBA Master drives the read data and asserts the read data valid signal. It continuously drives the read data and asserts the read data valid signal until the requester accepts the read data. The requester indicates that it is accepting read data by asserting the read data ready signal in the cycle when it accepts the read data.

The core is delivered as a synthesizeable RTL Verilog model. Deliverables include:

- RTL Verilog source code model of the core
- Verilog testbench and test cases
- Synthesis scripts examples
- Complete detailed documentation and training class notes

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