AU-B1000: AMBA AHB Bus Arbiter and Decoder Core

The AU-B1000 AMBA AHB Bus Arbiter and Decoder provides the bus arbiter and slave select decoder for the AMBA AHB Bus. It is fully pipelined for highest throughput and performance. The full set of sixteen AMBA Bus masters and sixteen AMBA Bus slaves is supported. The AMBA AHB Bus Arbiter/Decoder is available as a synthesizable Verilog model from Aurora VLSI, Inc. Contact CustomerService@auroravlsi.com.

Arbitration to choose the next bus master uses a round robin arbitration algorithm. This ensures that no master gets starved. When a master has locked the bus, the round robin arbitration is overridden and the master with the lock retains highest priority to the bus.

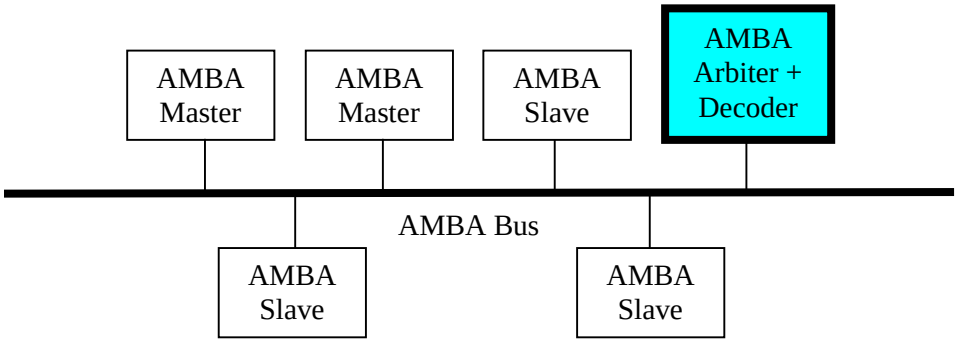
The AMBA AHB Bus Arbiter/Decoder contains sixteen programmable address registers- one address register per slave. These registers hold the base address and size of each slave's address space. Typically, other blocks of an SOC external to the AMBA AHB Bus Arbiter/Decoder, also need slave address space information. Therefore, contents of these registers are available as outputs from the AMBA AHB Bus Arbiter/Decoder.

The sixteen AMBA Bus masters are Master 0 through Master 15. Slave 0 through Slave 15 are the sixteen AMBA Bus slaves. The AMBA AHB Bus Arbiter/Decoder contains a default master- Master 0, and a default slave- Slave 0. Users may optionally replace the default master and/or default slave with their own default master and/or default slave.

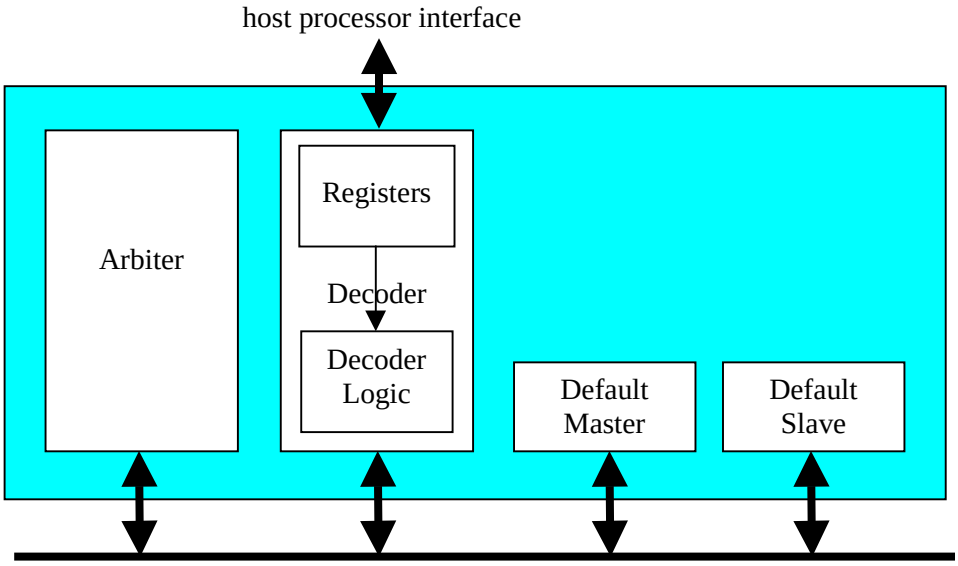
AMBA AHB Bus Arbiter/Decoder features are summarized:

- AMBA AHB Bus arbiter function
- AMBA AHB Bus decoder function
- 16 AMBA Bus masters
- 16 AMBA Bus slaves
- Fully pipelined for highest throughput
- Round robin arbitration
- 16 slave address registers- one register per slave
  - Base address of the slave's address space
  - Size of the slave's address space
- Default master- Master 0
- Default slave- Slave 0
- User can optionally supply the default master and/or default slave

The AMBA AHB Bus Arbiter/Decoder is shown in an AMBA Bus system in the figure below.



A block diagram of the AMBA AHB Bus Arbiter/Decoder is shown below.



The Arbiter block monitors the AMBA Bus for requests and chooses the master with highest priority request as the next AMBA bus transaction master. If there are no requests, the Default Master is chosen as the master to drive the next AMBA Bus transaction.

The Decoder block generates the select lines that steer the target slave's response onto the AMBA Bus. To do this, the Decoder block monitors the transaction address and decodes it by matching it to the slave base addresses stored in the Registers. The host processor writes these Registers to set up each slave's address space. If the Decoder encounters an address that does not match any of the slave address ranges, the Default Slave is chosen as the transaction target.

The core is delivered as a synthesizeable RTL Verilog model. Deliverables include:

- RTL Verilog source code model of the core
- Verilog testbench and test cases
- Synthesis scripts examples
- Complete detailed documentation and training class notes