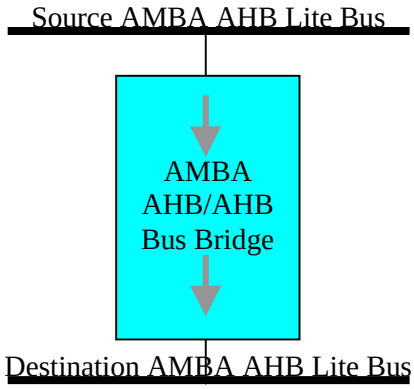
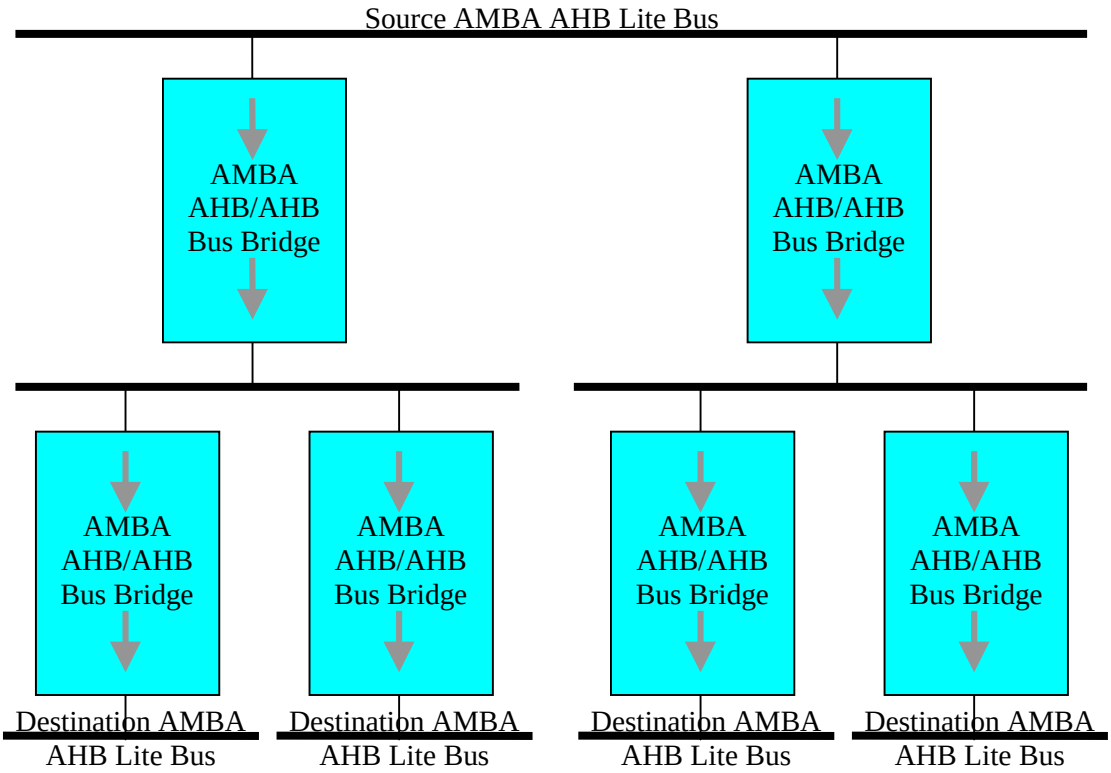
AU-B0003: AMBA AHB/AHB Bus Bridge Core

The AMBA AHB/AHB Bus Bridge is a unidirectional bridge between two AMBA AHB lite buses. It drives a transaction from a source AMBA AHB lite bus to a destination AMBA AHB lite bus. An AMBA AHB lite bus is an AMBA AHB bus that supports the OKAY and ERROR AMBA bus responses, but does not support the RETRY and SPLIT AMBA bus responses. The AMBA AHB/AHB Bus Bridge is available as a synthesizable Verilog model from Aurora VLSI, Inc. Contact CustomerService@auroravlsi.com.



Unidirectional AMBA AHB Lite Bus Bridge



Multiple Layers of AMBA AHB Lite Buses

The AMBA AHB/AHB Bus Bridge supports up to 64 address spaces on the destination AMBA bus. These may be the address spaces of AMBA slaves on the destination bus. Alternatively, they may be address spaces "behind" another bridge on the destination AMBA bus.

The AMBA AHB/AHB Bus Bridge supports all AMBA AHB data sizes, transaction types, and burst types. Additionally, the AMBA buses can be configured to be either 32 bit or 64 bit AMBA buses. Transaction information is passed from the source AMBA bus to the destination AMBA bus without modification. A write buffer is included to minimize write data wait states. On reads, depending to the burst type, the AMBA AHB/AHB Bus Bridge prefetches data on the destination AMBA bus so that the peak data rate can be maintained during bursts.

The source AMBA bus clock and destination AMBA bus clock may be the same clock or separate asynchronous clocks.

AMBA AHB/AHB Bus Bridge features are summarized:

- Unidirectional source AMBA bus to destination AMBA bus bridge function
- Multiple master, multiple slave source AMBA bus
- Single AMBA bus bridge master, multiple slave destination AMBA bus
- 32 bit or 64 bit AMBA buses- user configurable
- 64 destination AMBA bus address spaces
- Supports all AMBA bus transaction types
- Supports all AMBA bus burst types
- Supports AMBA bus data sizes of 1, 2, 4, and 8 bytes
- Supports OKAY and ERROR AMBA response types
- AMBA bus transaction address, read/write, transaction type, burst type, and data size are passed from the source AMBA bus to the destination AMBA bus without modification
- Write buffer to minimize AMBA bus wait states
- Read data prefetching to minimize AMBA bus wait states
- Synchronous or asynchronous source and destination AMBA AHB bus clocks
- Zero latency with synchronous clocks
- Low latency with asynchronous clocks

The core is delivered as a synthesizeable RTL Verilog model. Deliverables include:

- RTL Verilog source code model of the core
- Verilog testbench and test cases
- Synthesis scripts examples
- Complete detailed documentation and training class notes