AU-B0000: AMBA AHB Bus Core

The AU-B0000 AMBA AHB Bus provides the muxes that implement the AMBA AHB Bus as described in the "AMBA Specification 2.0". The read and write data widths are user configurable to either 32 bits or 64 bits. The number of AMBA Bus masters and slaves connected to the AMBA AHB Bus is also user configurable, up to sixteen of each. The AMBA AHB Bus is available as a synthesizable Verilog model from Aurora VLSI, Inc. Contact CustomerService@auroravlsi.com.

The sixteen AMBA Bus masters are Master 0 through Master 15. Slave 0 through Slave 15 are the sixteen AMBA Bus slaves. The AMBA Bus contains a default master- Master 0, and a default slave- Slave 0. The user may optionally replace the default master and/or default slave with his own default master and/or default slave.

Each AMBA Bus master and AMBA Bus slave has a dedicated interface to the AMBA AHB Bus.

The AMBA AHB Bus connects seamlessly to the AMBA AHB Bus Arbiter/Decoder, AMBA AHB/APB Bus Bridge, AMBA AHB Masters, and AMBA AHB Slaves from Aurora VLSI.

AMBA AHB Bus features are summarized:

- AMBA AHB Bus
- 32 bit or 64 bit data widths- user configurable
- 1 to 16 AMBA Bus masters- user configurable
- 1 to 16 AMBA Bus slaves- user configurable
- Default master- Master 0
- Default slave- Slave 0
- User can optionally supply the default master and/or default slave
- Seamless connections to AMBA AHB Master, AMBA AHB Slave, AMBA AHB Bus Arbiter/Decoder, and AMBA AHB/APB Bus Bridge from Aurora VLSI.

The core is delivered as a synthesizeable RTL Verilog model. Deliverables include:

- RTL Verilog source code model of the core
- Verilog testbench and test cases
- Synthesis scripts examples
- Complete detailed documentation and training class notes