AU-A7540: Floating Point Core

The AU-A7540 Floating Point Core provides IEEE754-1985 compliant single and double precision floating point. It implements floating point addition, subtraction, multiplication, division, conversions, comparisons, negation, and absolute value in hardware. IEEE754-1985 compliant results are completely computed by hardware. The Floating Point Core is available as a synthesizable Verilog model from Aurora VLSI, Inc. Contact CustomerService@auroravlsi.com.

The Floating Point Core implements all four IEEE rounding modes- round to nearest, round to zero, round to positive infinity, and round to negative infinity. All five IEEE floating point exceptions are detected- invalid operation, underflow, overflow, inexact, and divide by zero.

The Floating Point Core handles denorm inputs in hardware. It also completely computes the rounded IEEE754 result in hardware, including any denorm, zero, infinity, or NaN result. The five floating point exception flags are delivered along with the result.

For highest performance, the FPU is pipelined and runs at frequencies up to 330 MHz (worst case slow) in .13u technologies.

Floating Point features are summarized:

- IEEE754-1985 floating point
- Fully compliant results for all floating point operations are computed in hardware
- Single and double precision
- Floating point operations include:
  - addition- single and double precision
  - subtraction- single and double precision
  - multiplication- single and double precision
  - division- single and double precision
  - float to float conversions- single to double, double to single
  - float to integer conversions- single/double to 32/64 bit integer
  - integer to float conversions- 32/64 bit integer to single/double
  - comparision- single and double precision
  - negation- single and double precision
  - absolute value- single and double precision
- Rounding modes
  - round to nearest
  - round to zero
  - round to positive infinity
  - round to negative infinity
- Exceptions detected- inexact, overflow, underflow, invalid, and divide by zero

The core is delivered as a synthesizeable RTL Verilog model. Deliverables include:

- RTL Verilog source code model of the core
- Verilog testbench and test cases
- Synthesis scripts examples
- Complete detailed documentation and training class notes